

FIG. 1

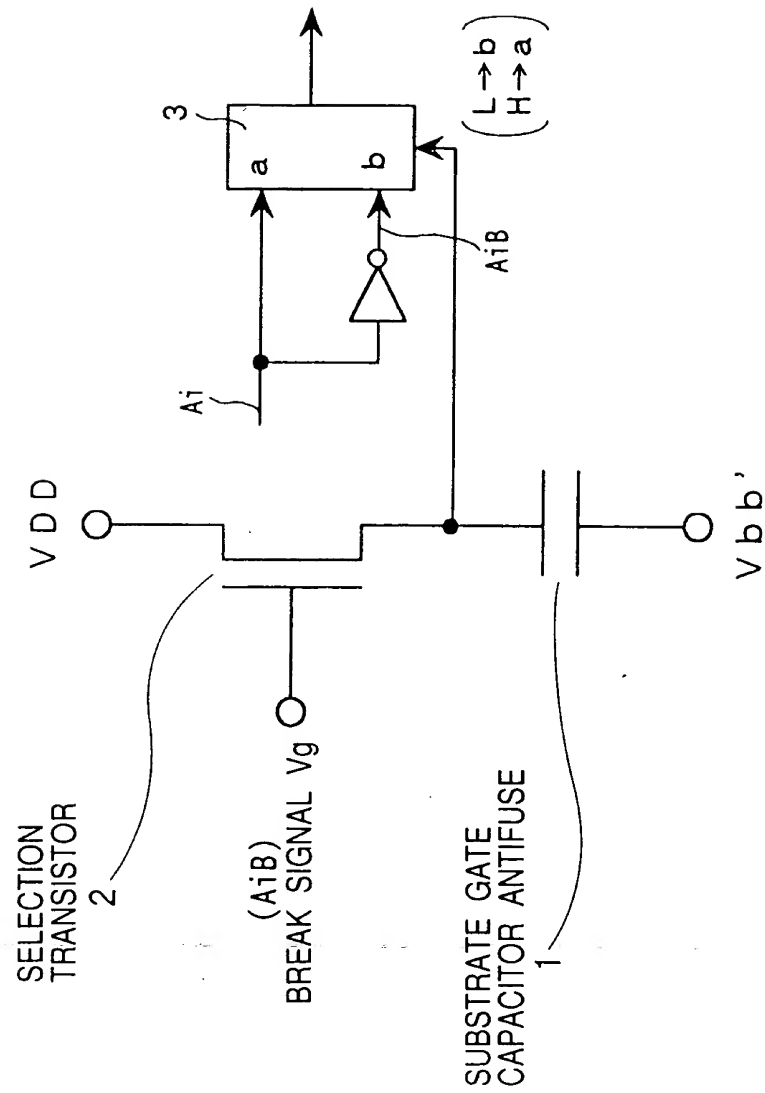


FIG. 2

FIG. 2

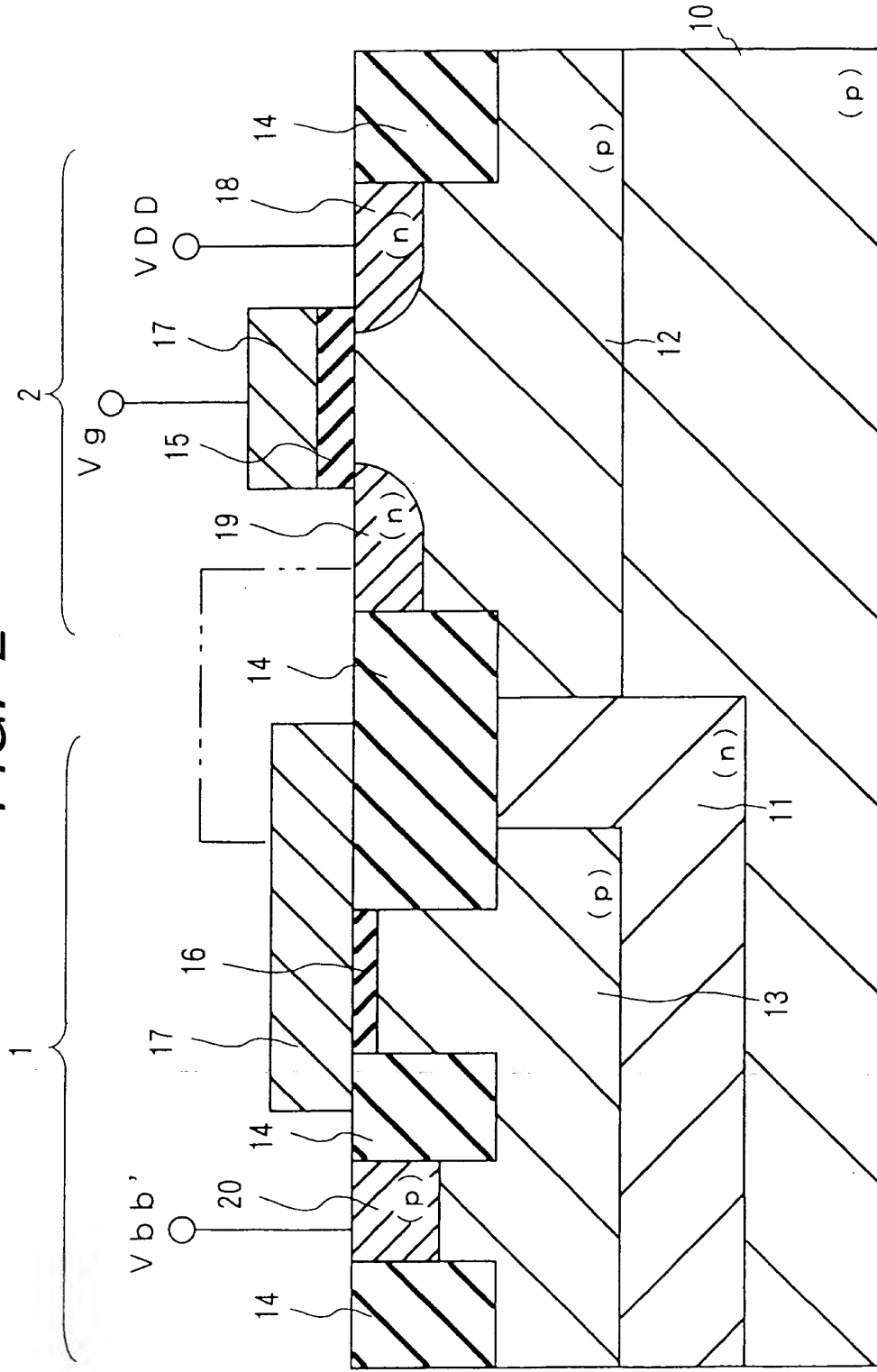


FIG. 3

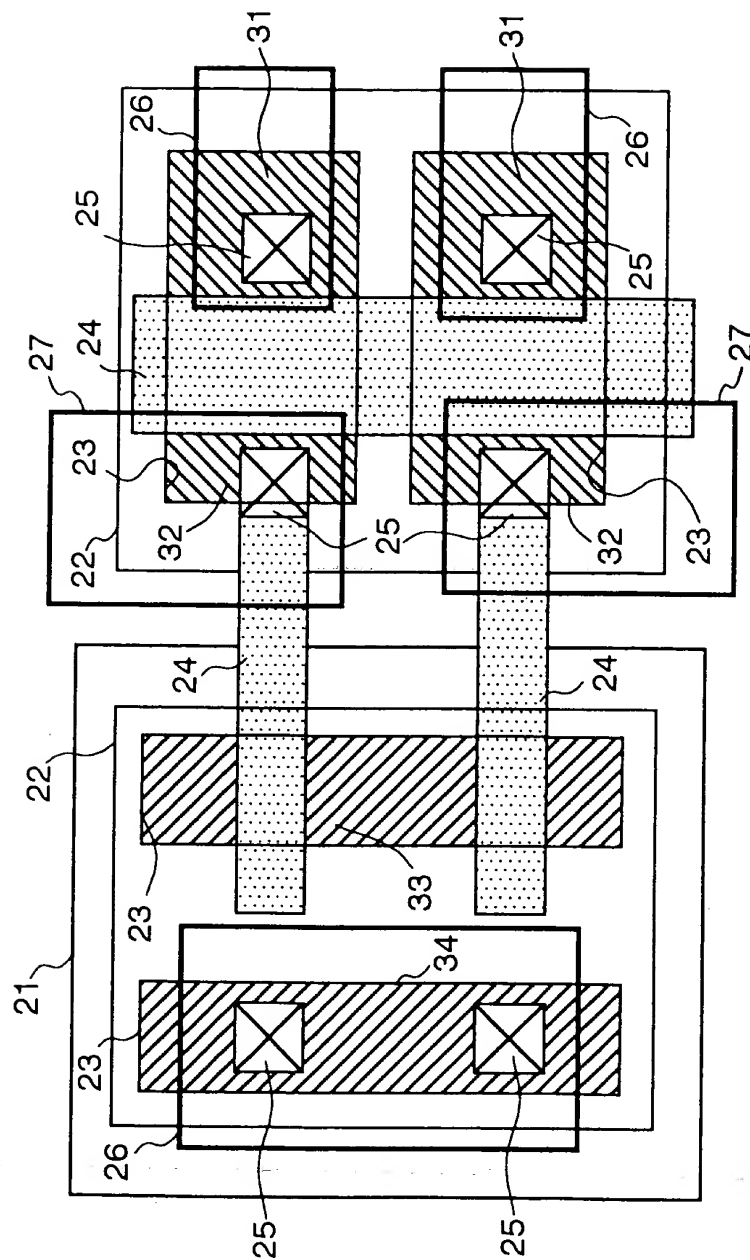


FIG. 4

FIG. 4

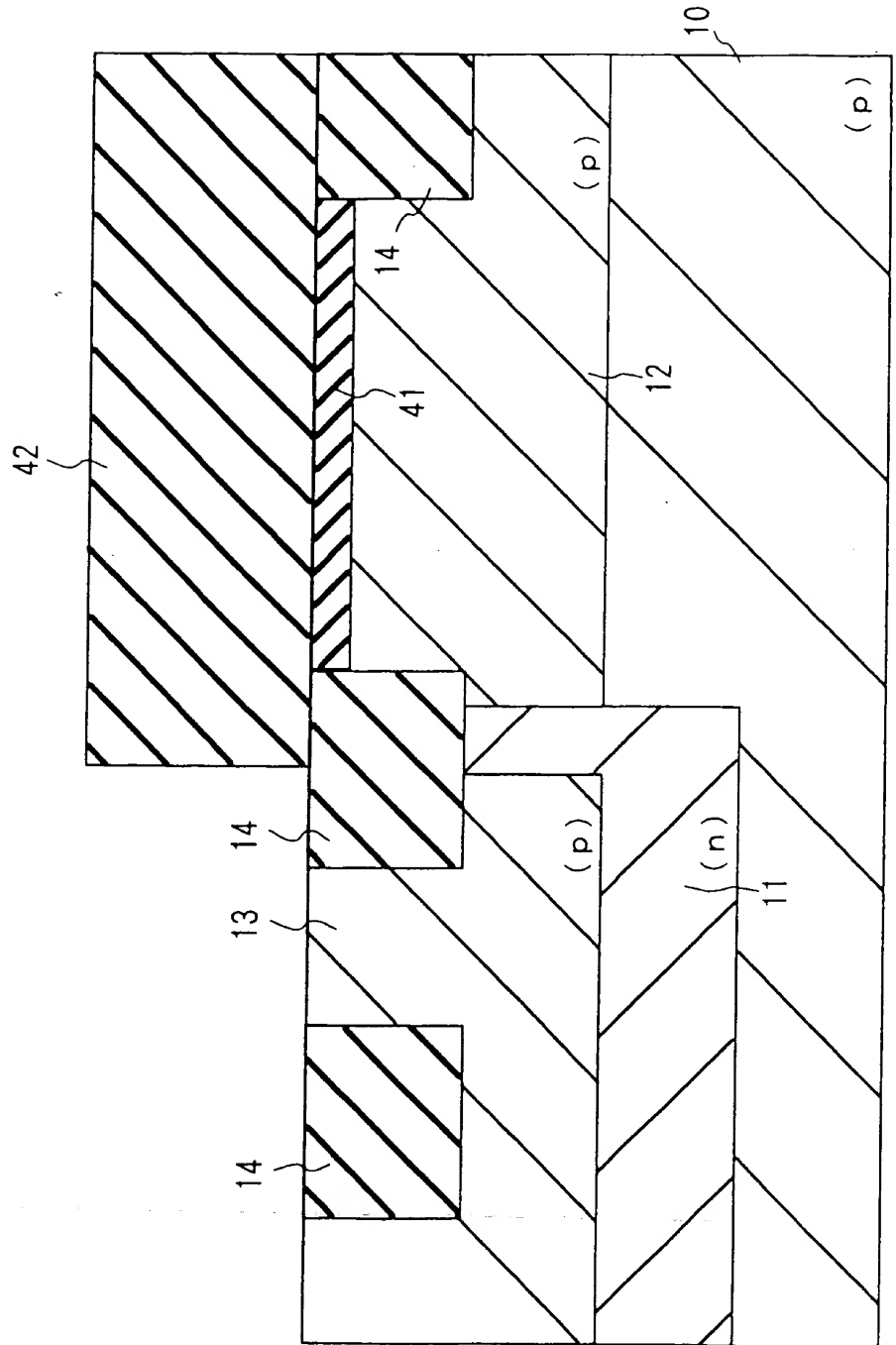


FIG. 5

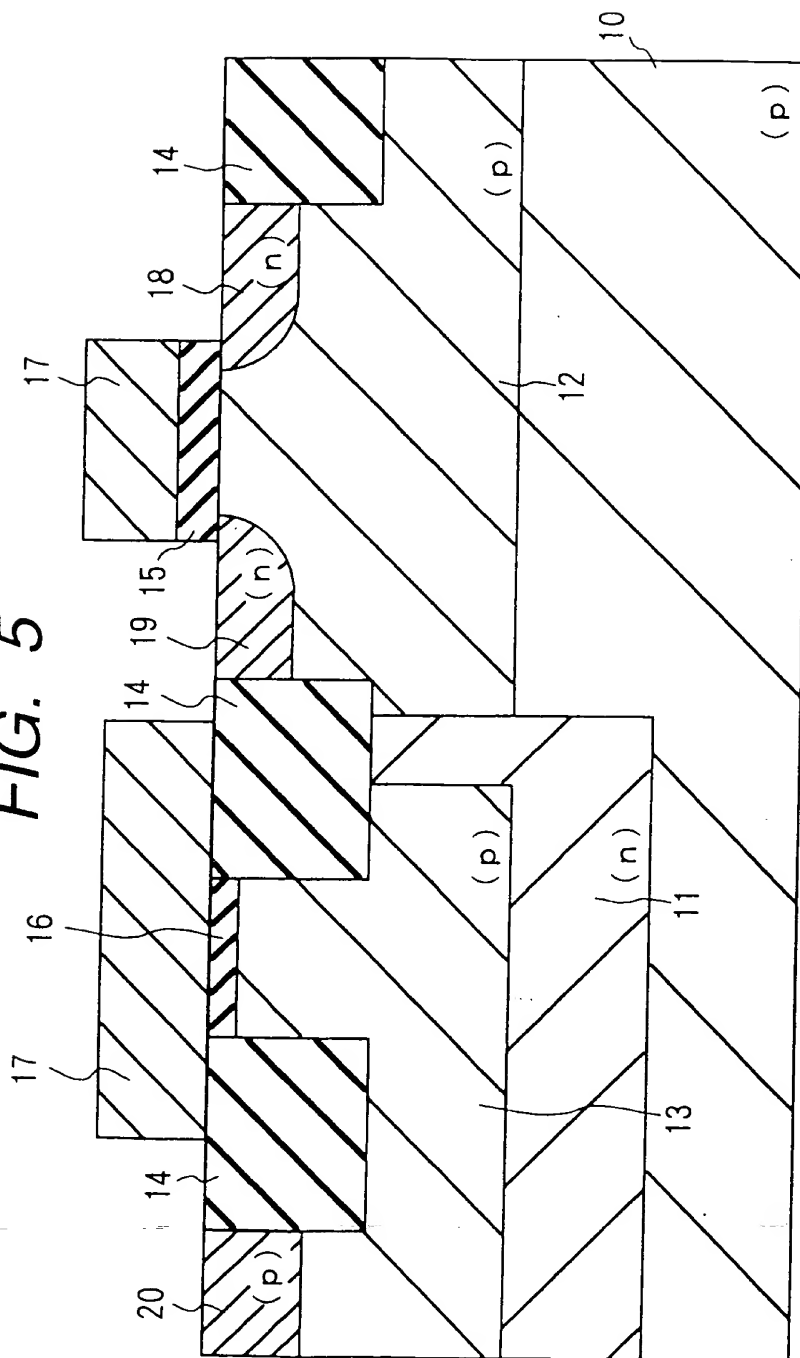


FIG. 6

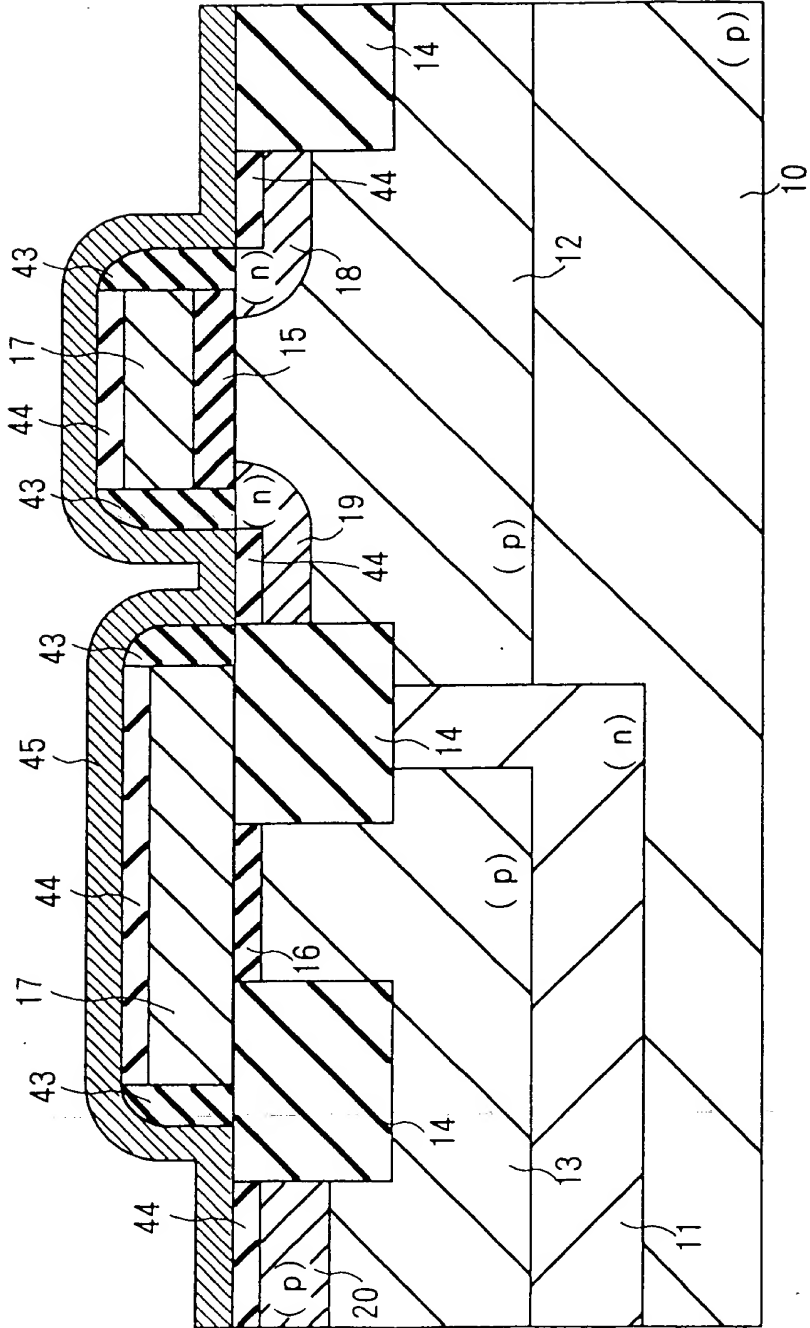


FIG. 8

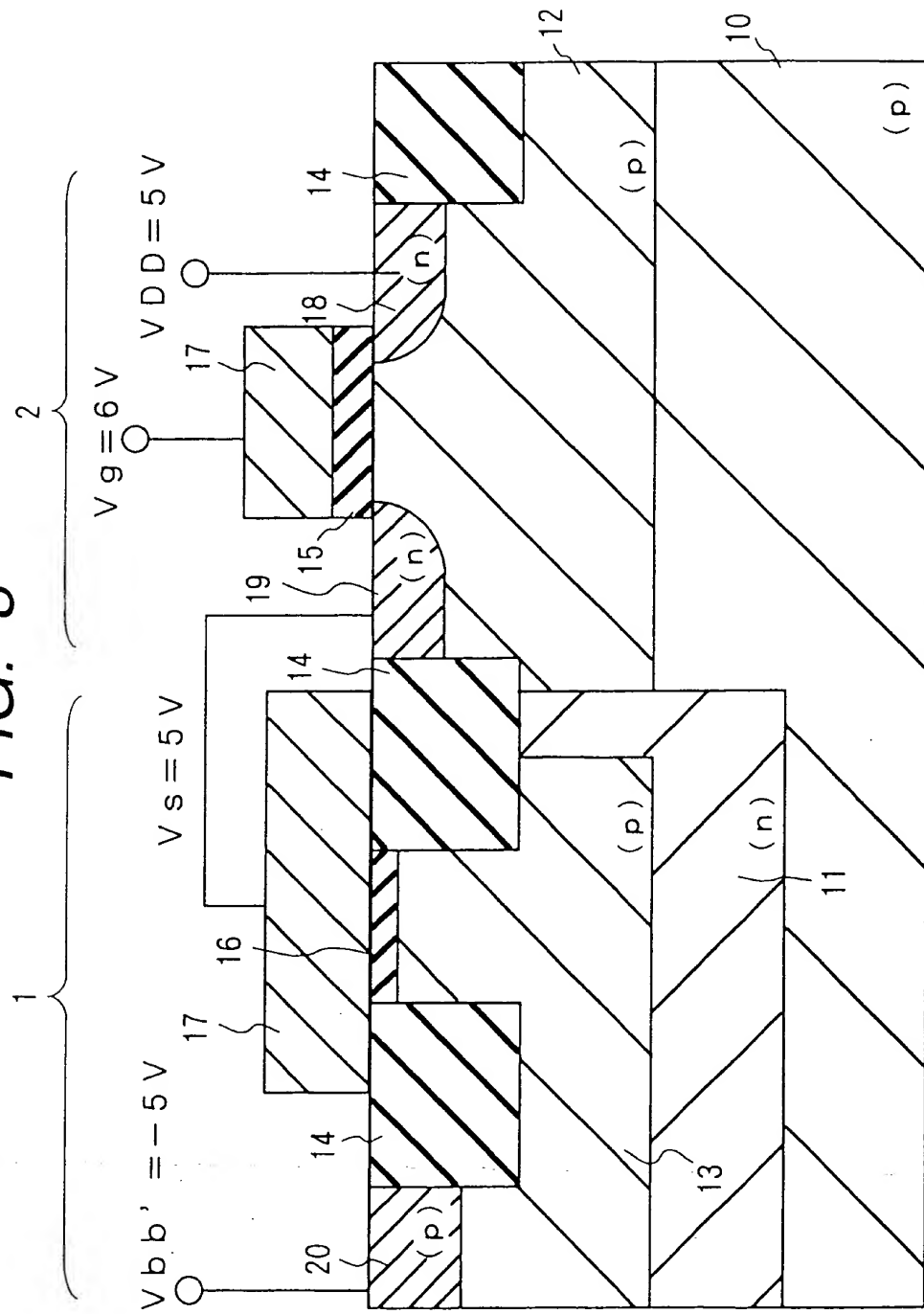


FIG. 9

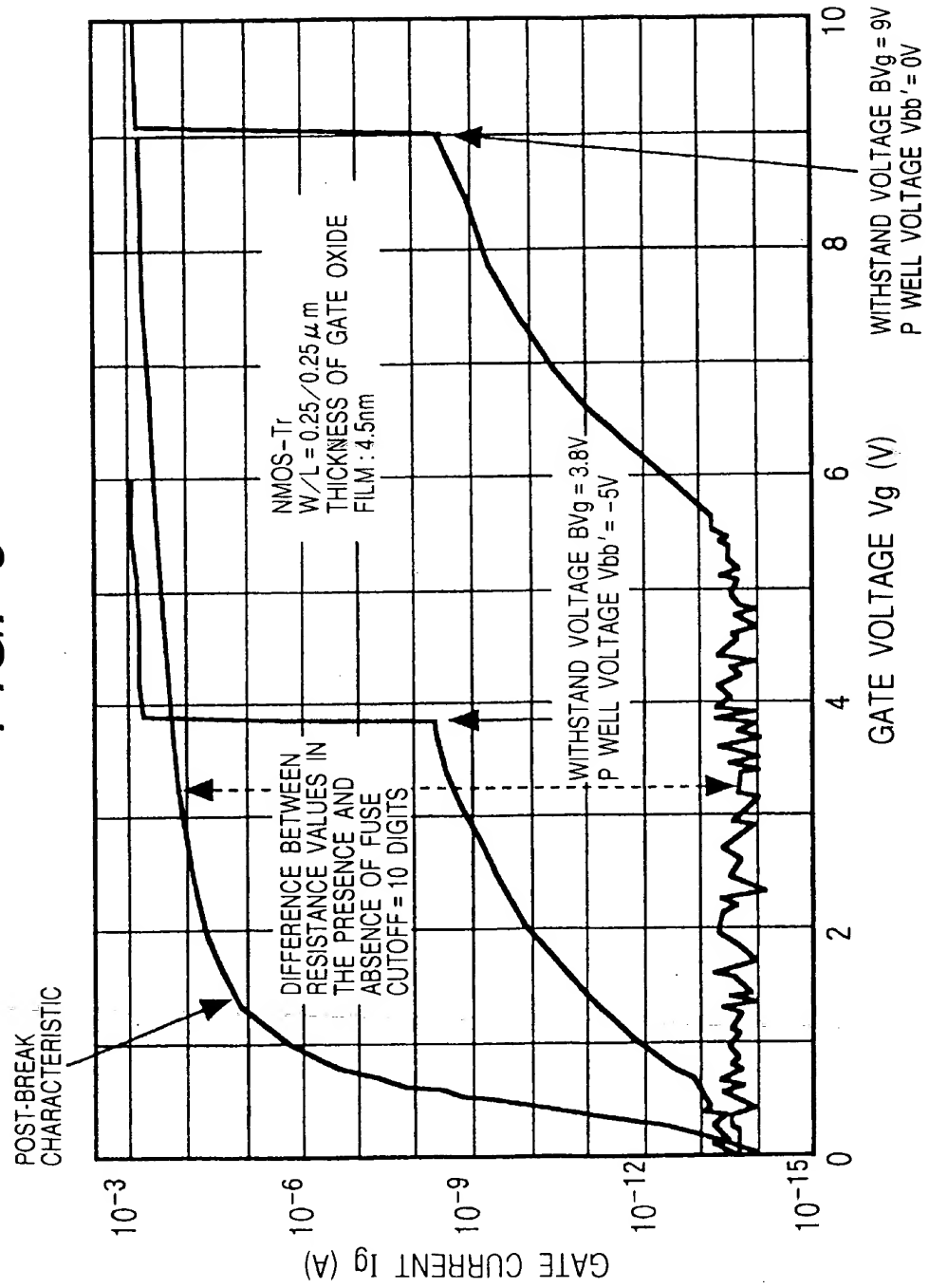


FIG. 10

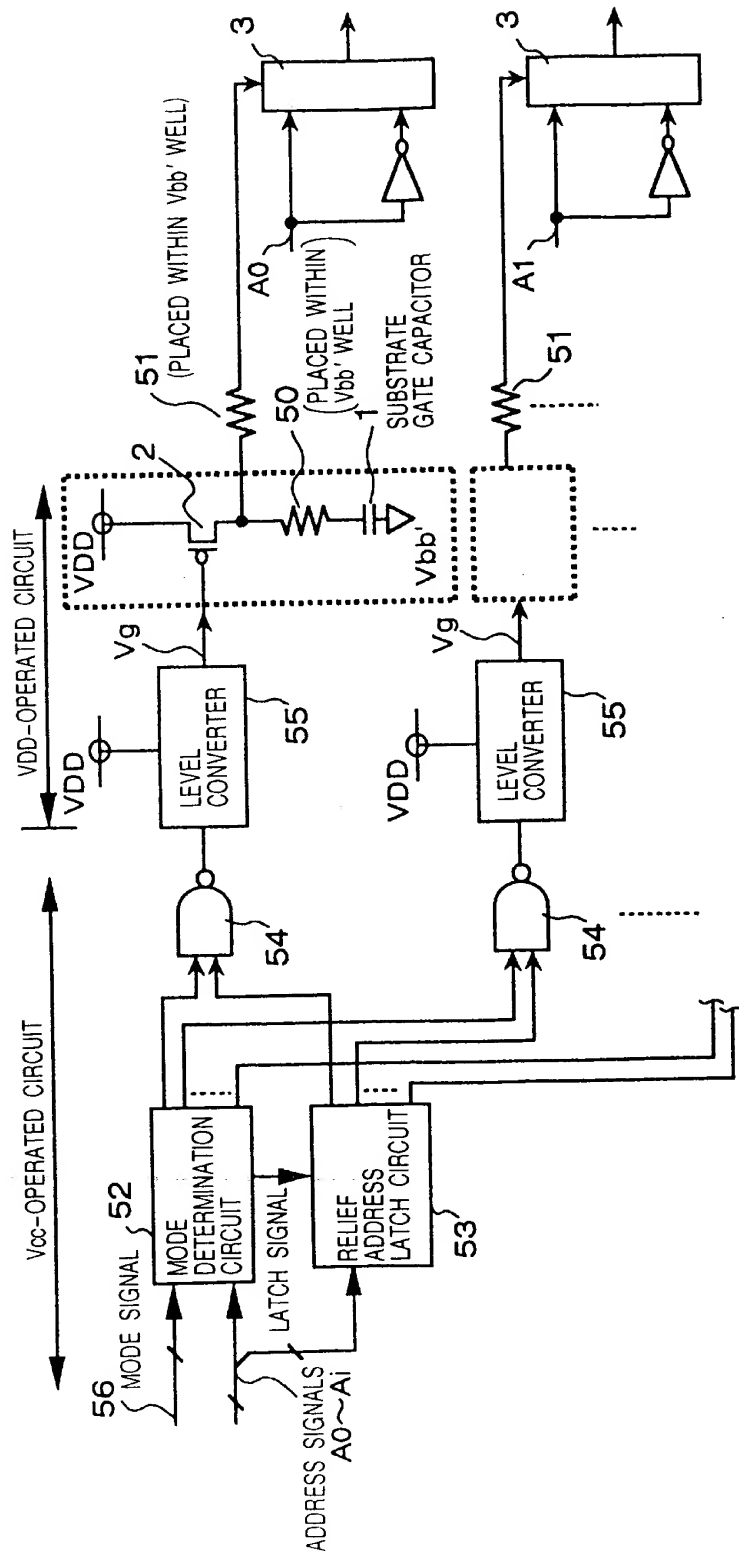


FIG. 11

FIG. 11

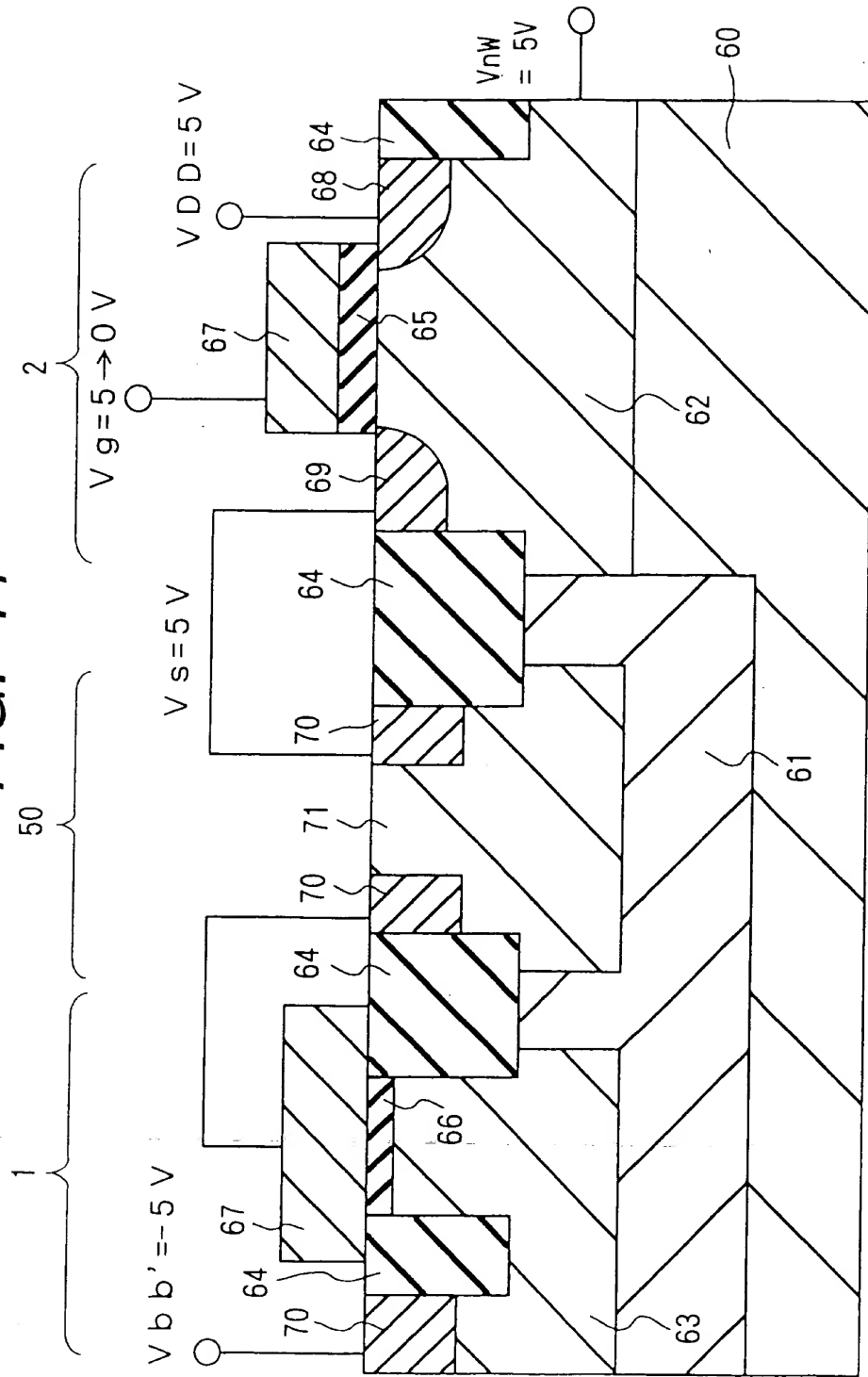
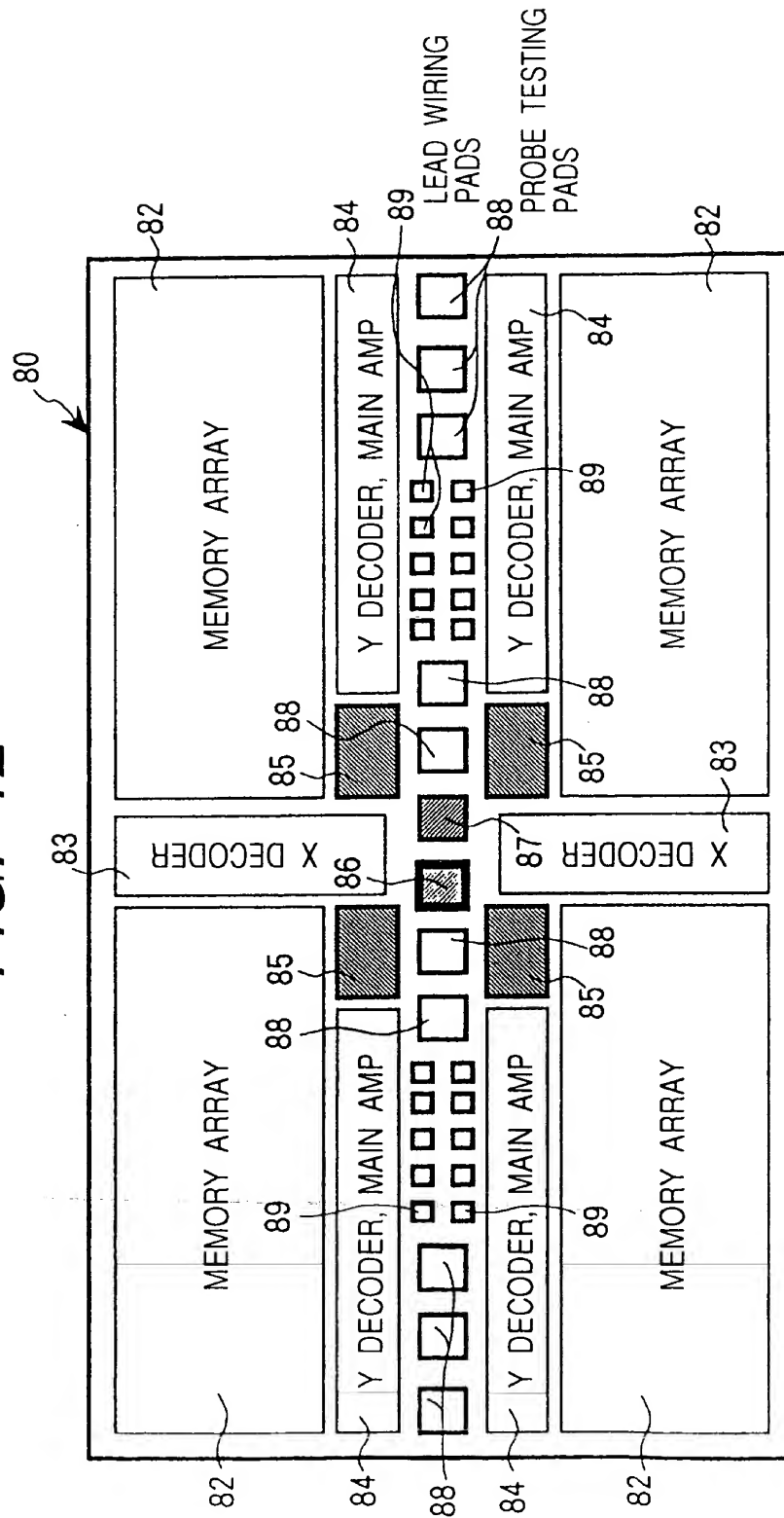


FIG. 12



85 : ANTIFUSE CIRCUIT	86 : VDD PAD APPLY VDD UPON DIELECTRIC BREAKDOWN FIX V _{cc} AFTER DIELECTRIC BREAKDOWN	87 : V _{bb} ' PAD APPLY V _{bb} ' UPON DIELECTRIC BREAKDOWN FIX V _{ss} AFTER DIELECTRIC BREAKDOWN
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FIG. 13

FIG. 13

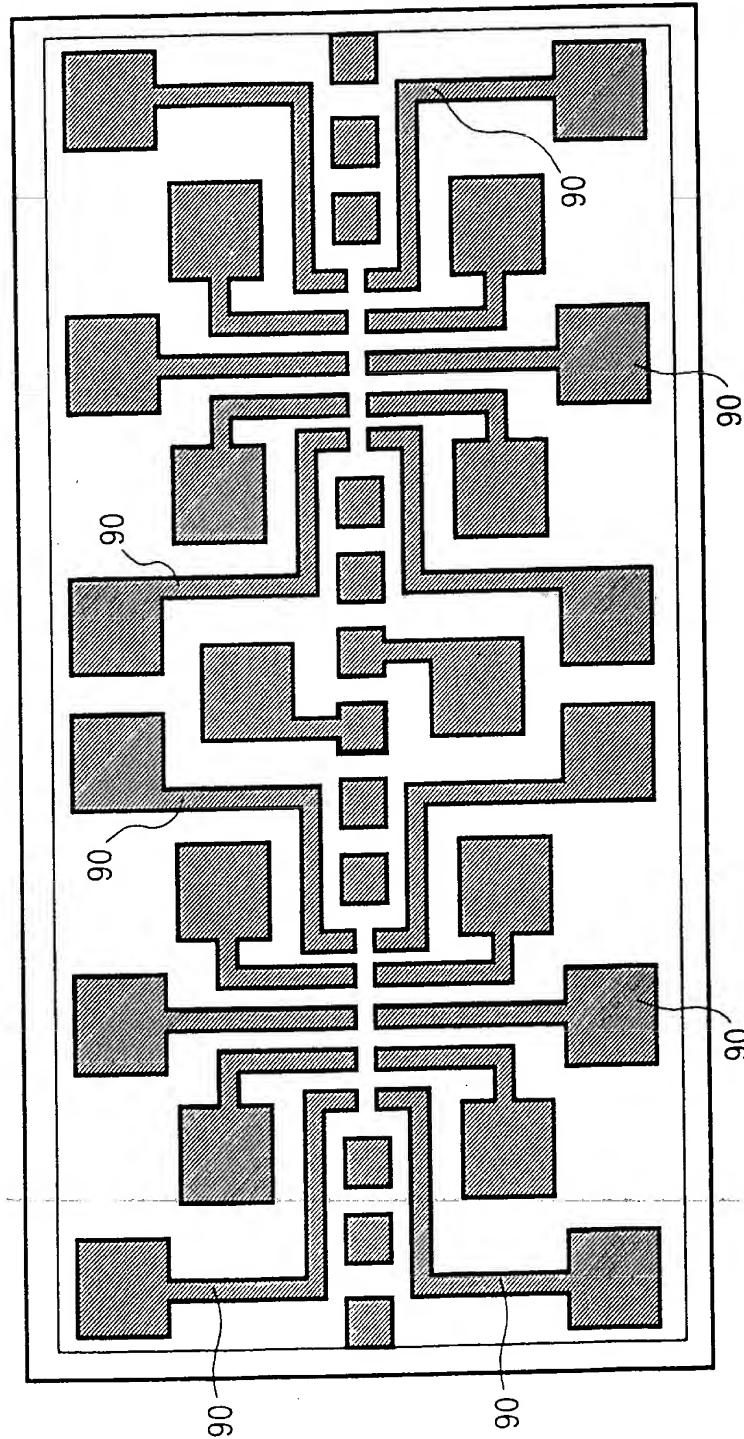
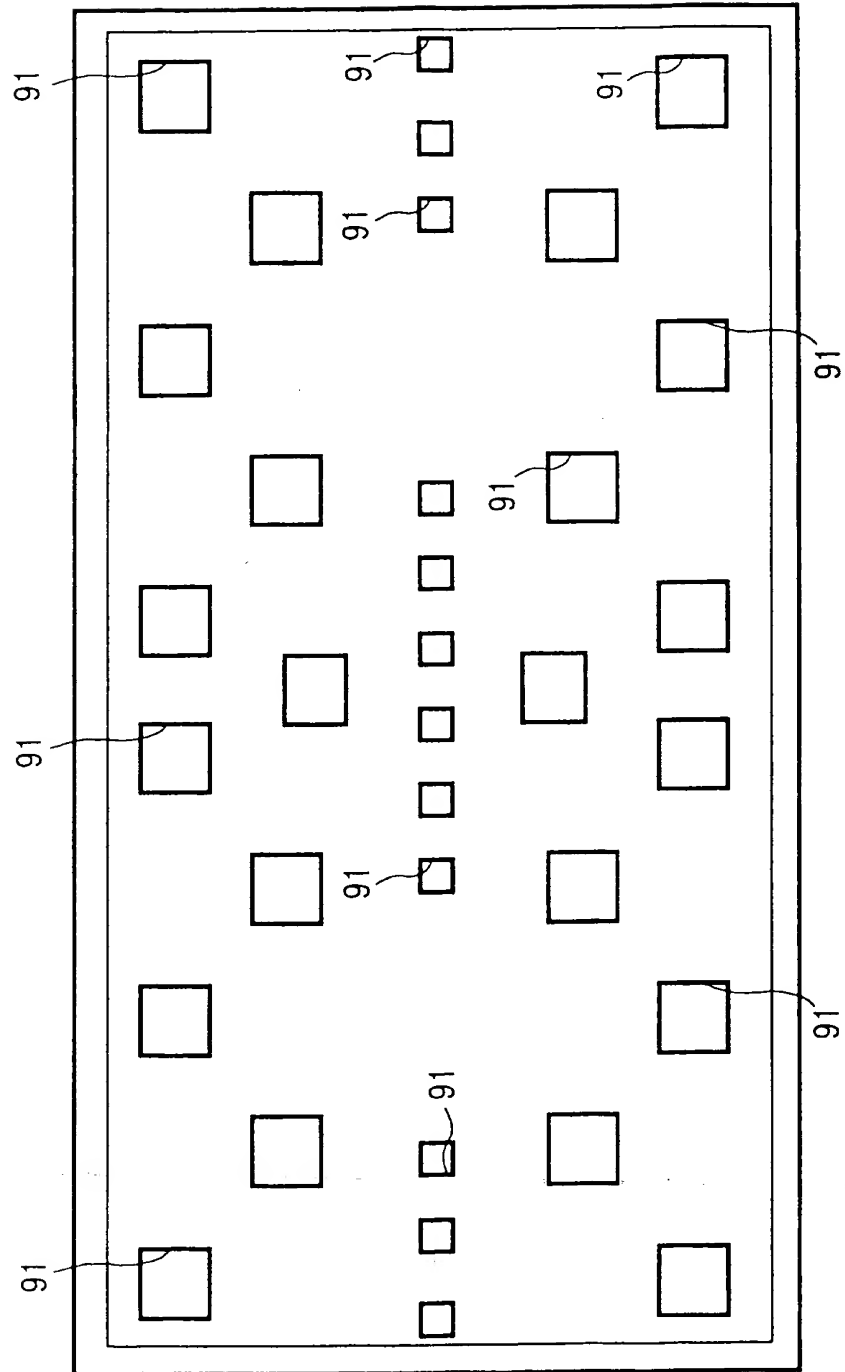


FIG. 14

FIG. 14



09/869274

15/38

09/869274

FIG. 15

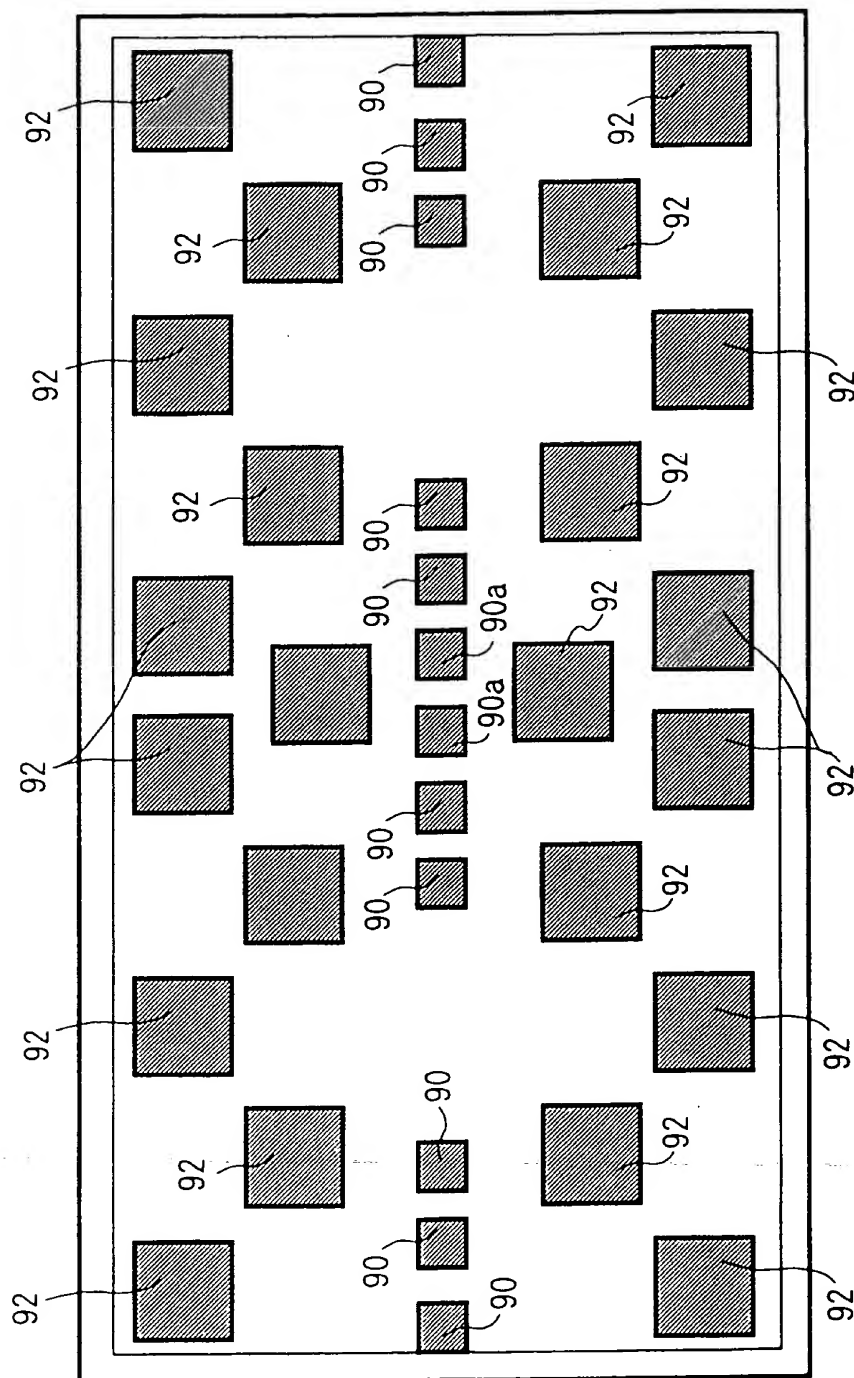


FIG. 16

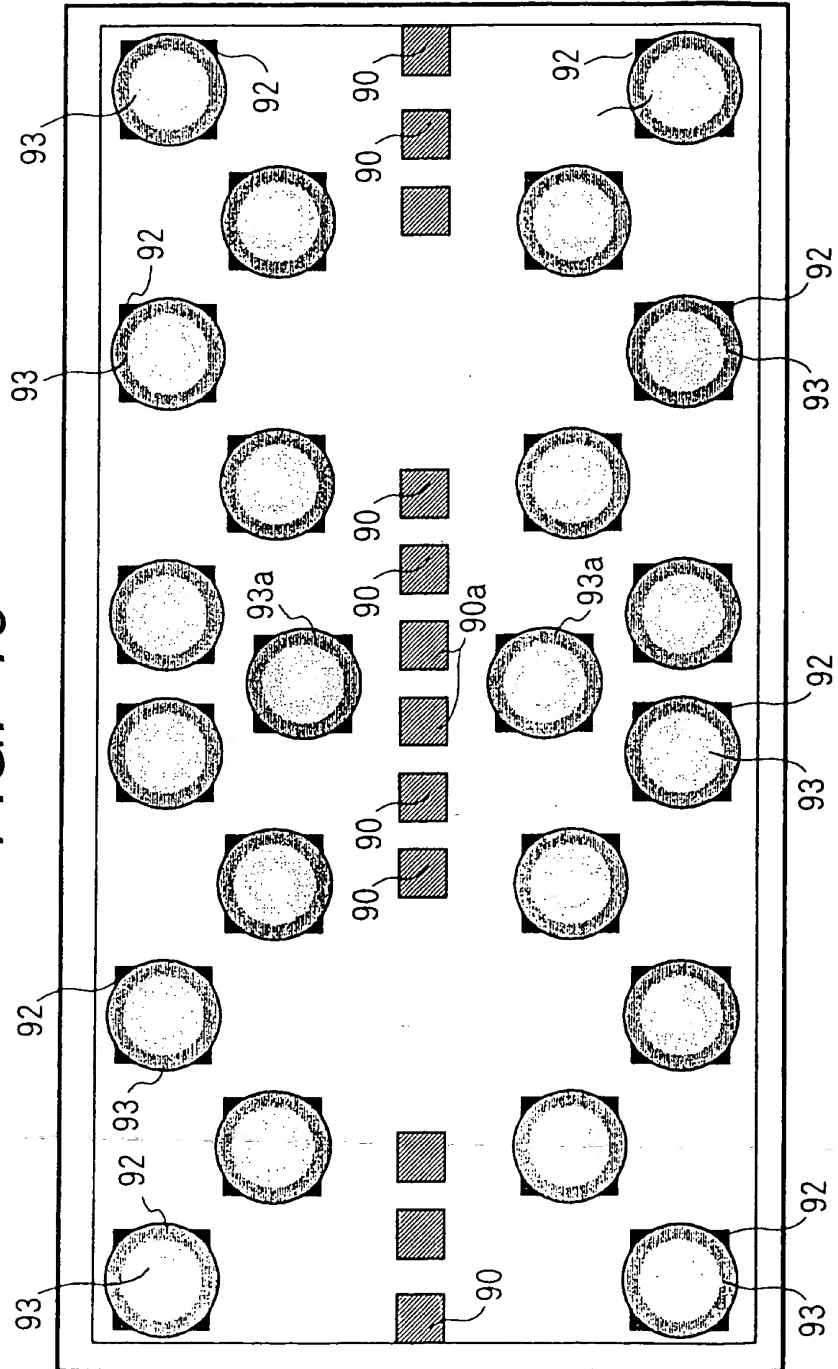


FIG. 17

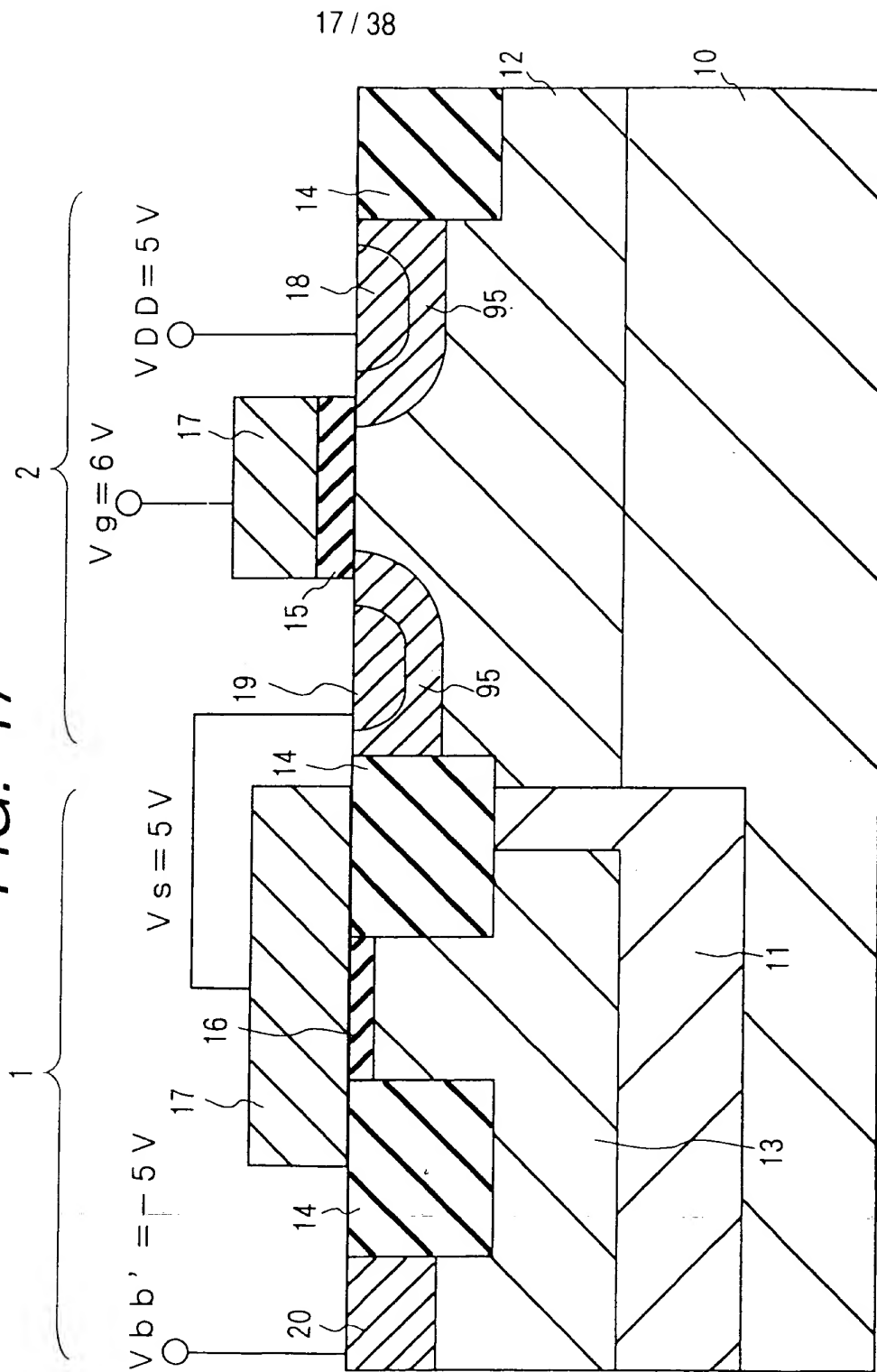


FIG. 18

FIG. 18

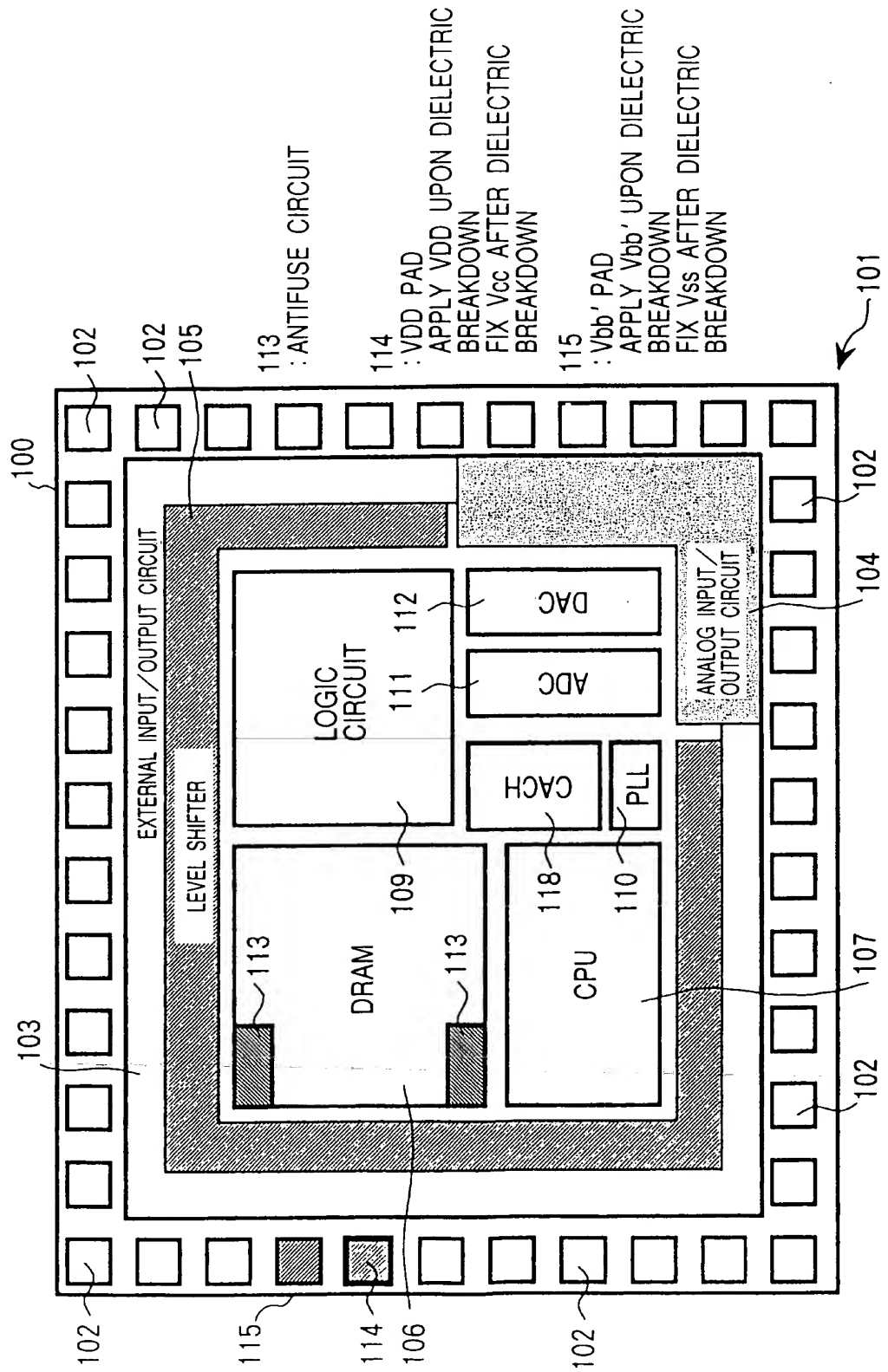


FIG. 19

FIG. 19

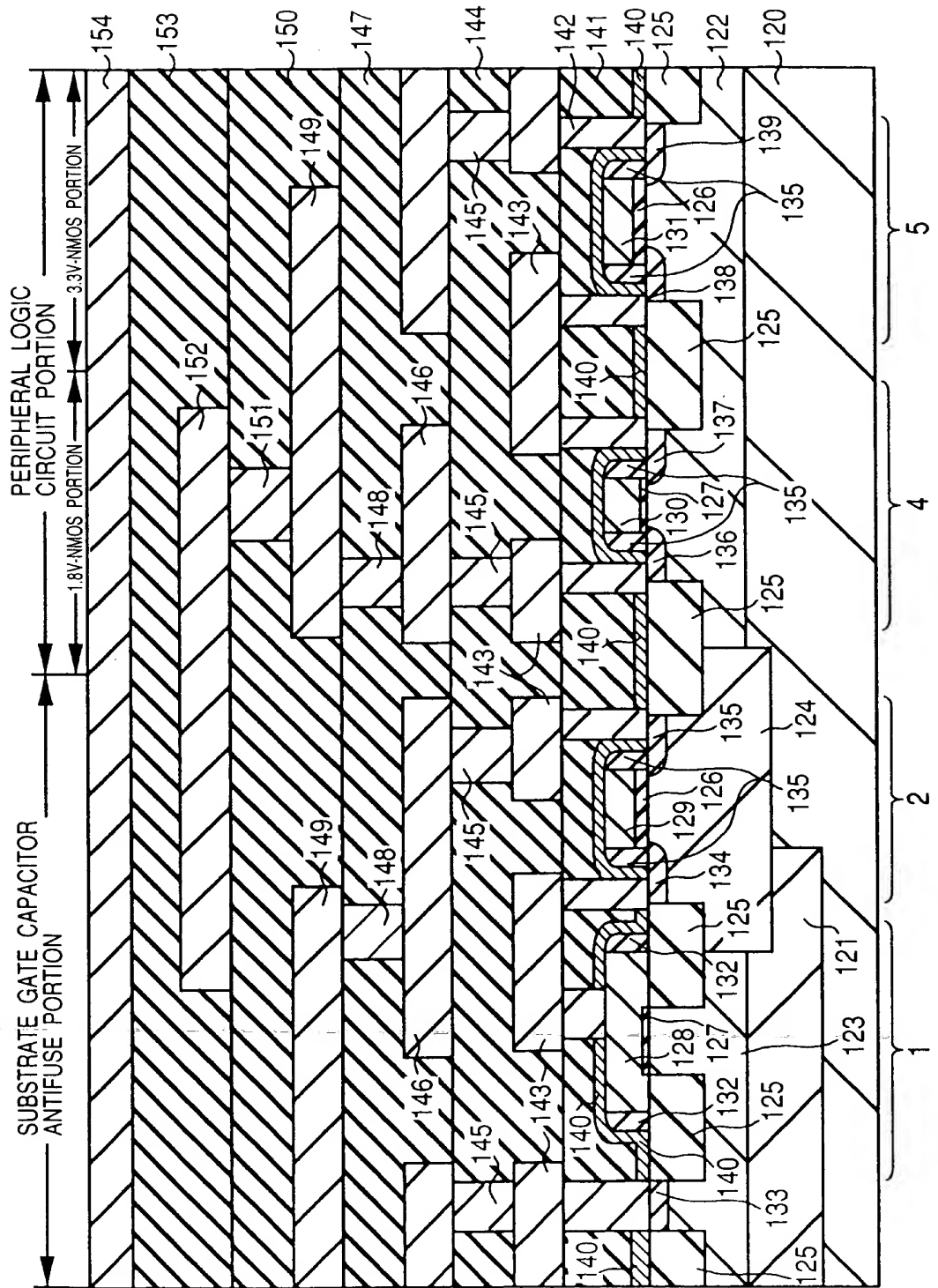


FIG. 20

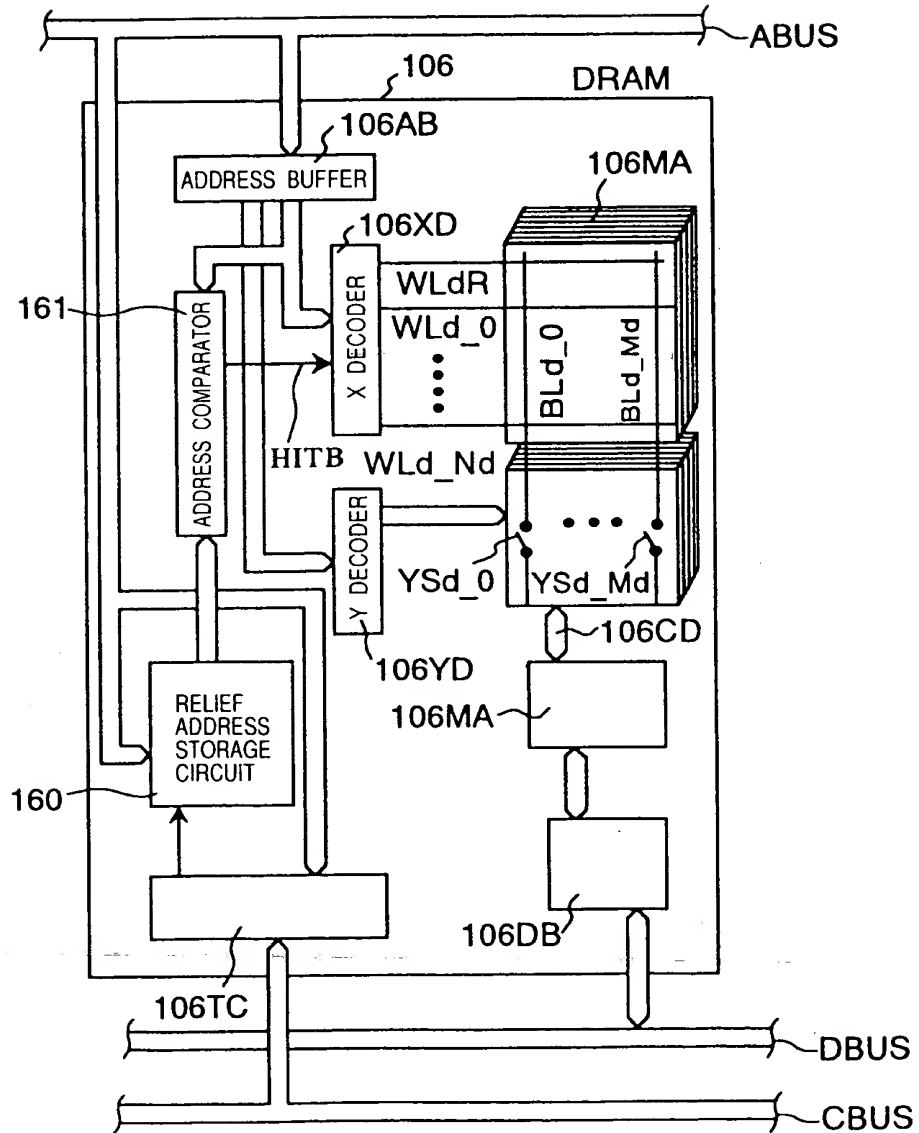


FIG. 21

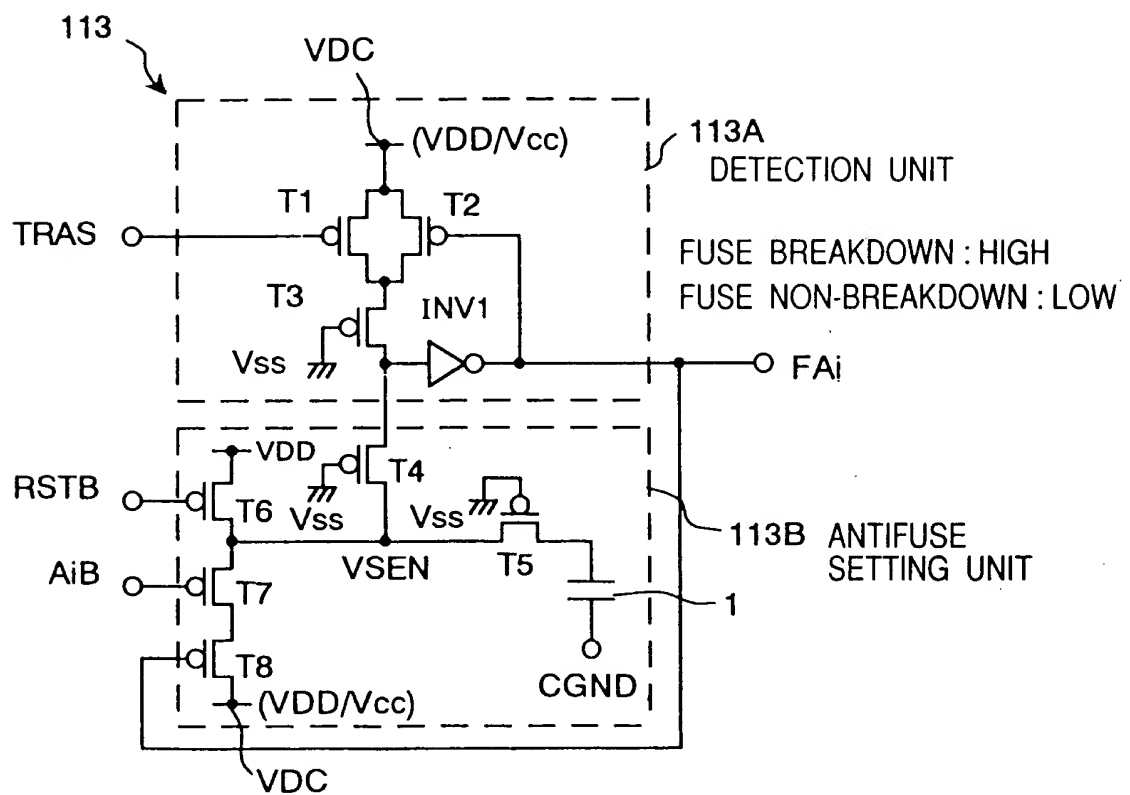


FIG. 22

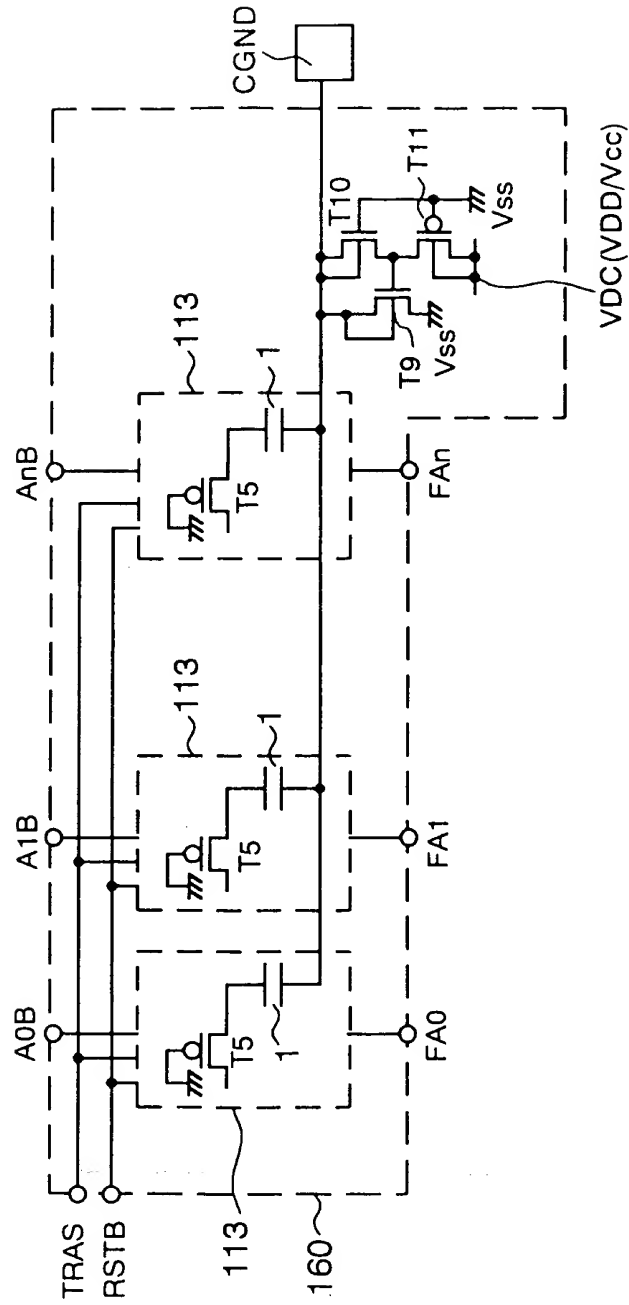
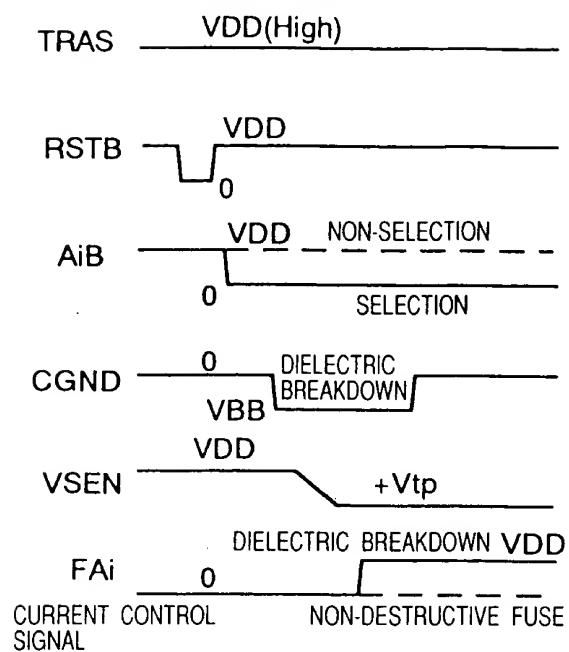


FIG. 23

(FUSE PROGRAM)

**FIG. 24**

(FUSE READOUT)

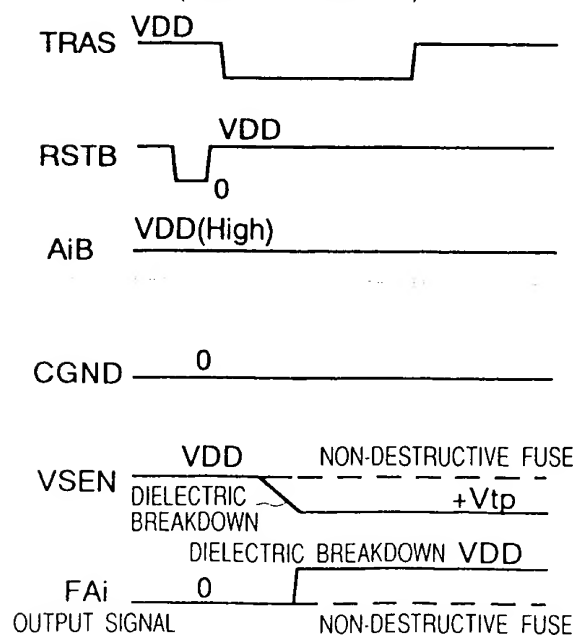


FIG. 25

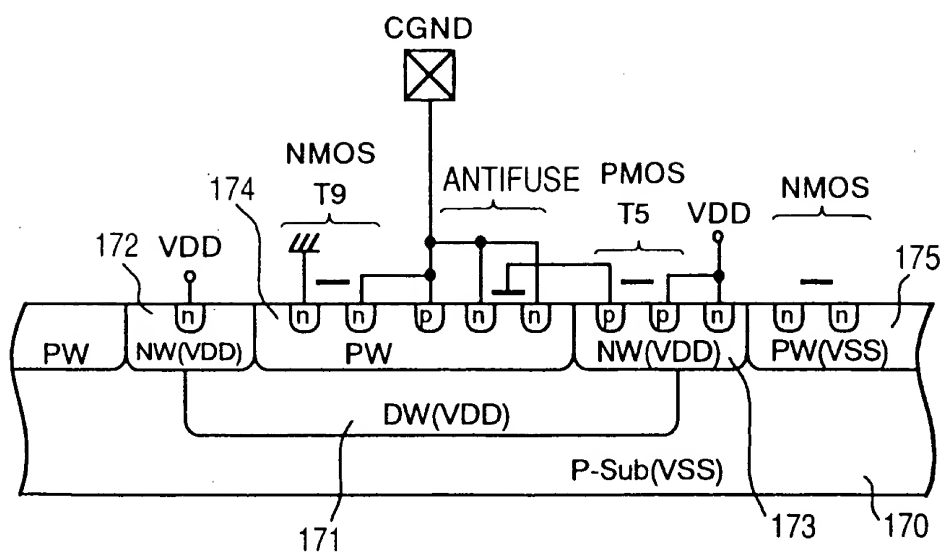


FIG. 26

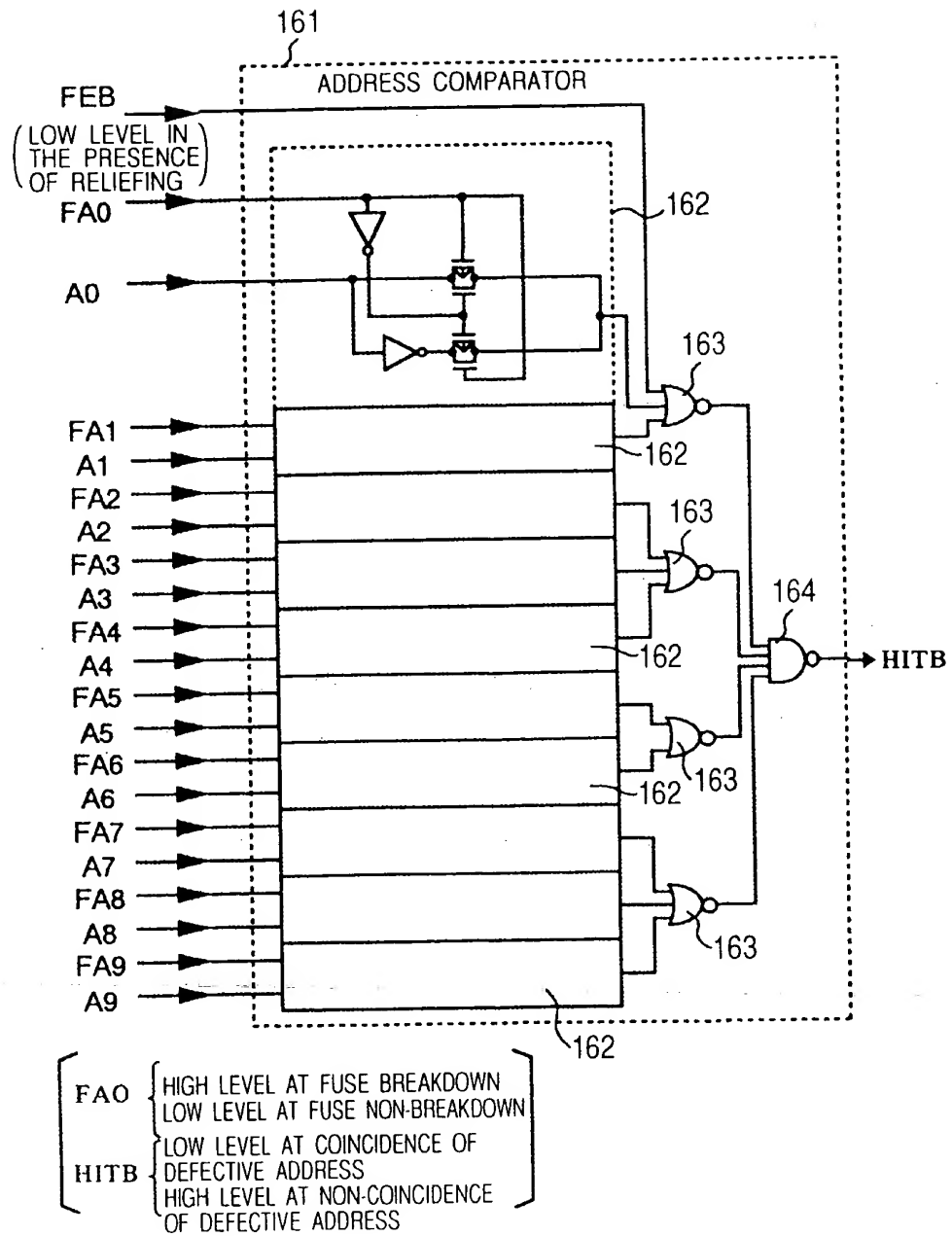


FIG. 27

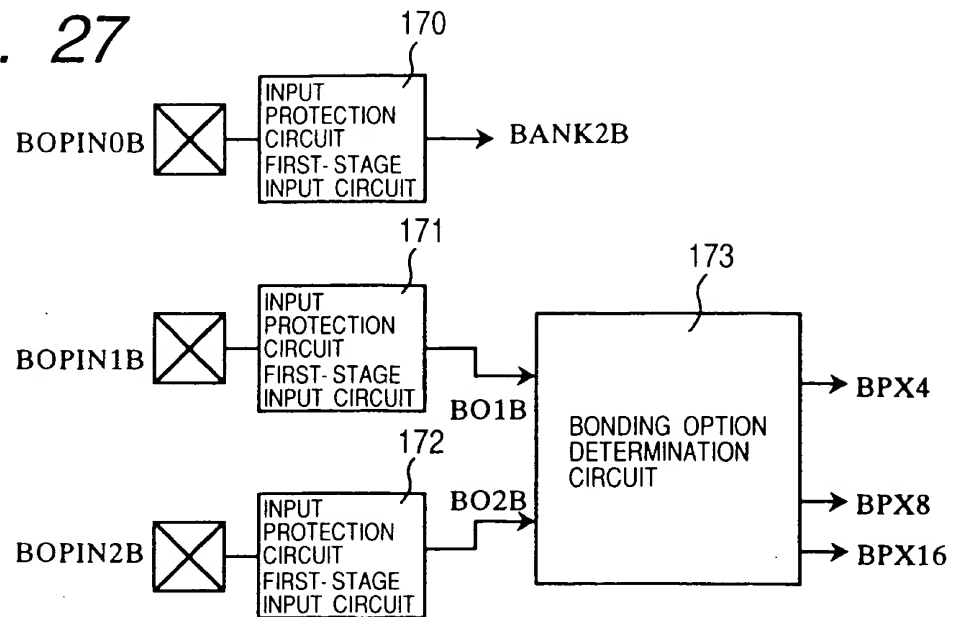


FIG. 28

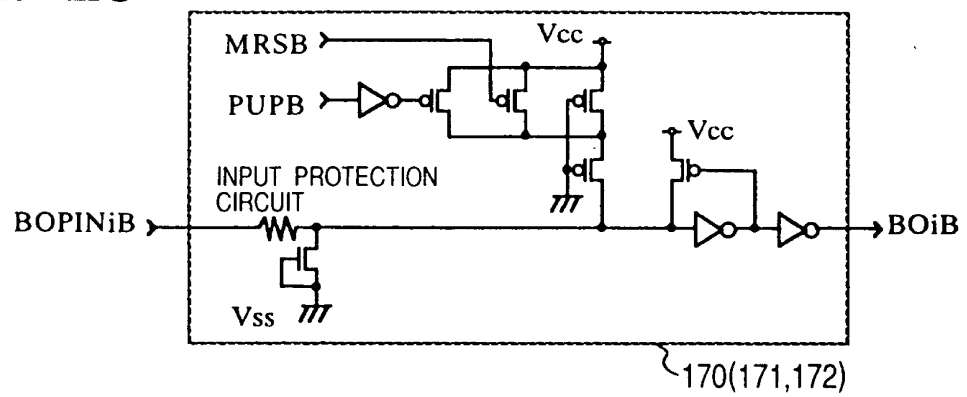


FIG. 29

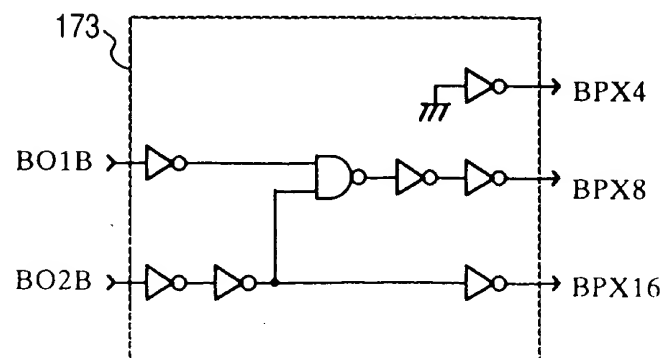
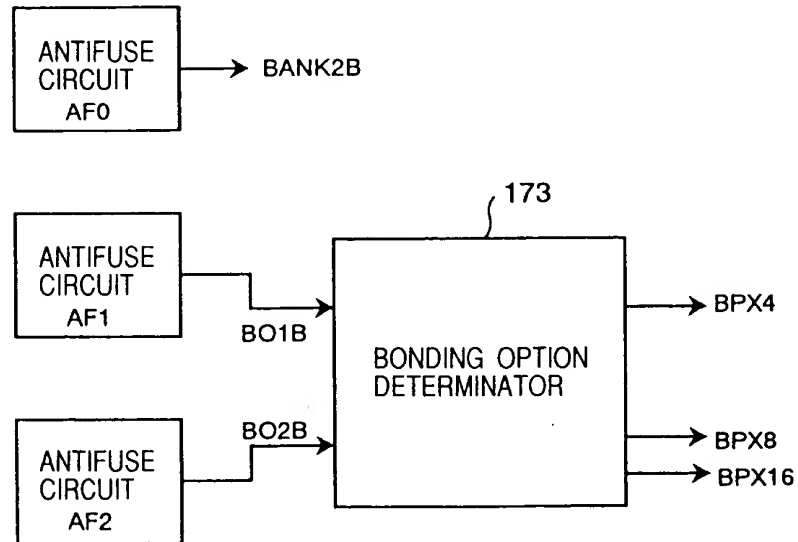


FIG. 30

LIST OF BONDING OPTION SPECIFICATIONS

SPECIFICATIONS	INPUT			OUTPUT			
	BOPIN0B	BOPIN1B	BOPIN2B	BNK2B	BPX4	BPX8	BPX16
4Bank / x4	Floating	VSS	Floating	'H'	'H'	'L'	'L'
4Bank / x8	Floating	Floating	Floating	'H'	'H'	'H'	'L'
4Bank / x16	Floating	Floating	VSS	'H'	'H'	'H'	'H'
2Bank / x4	VSS	VSS	Floating	'L'	'H'	'L'	'L'
2Bank / x8	VSS	Floating	Floating	'L'	'H'	'H'	'L'
2Bank / x16	VSS	Floating	VSS	'L'	'H'	'H'	'H'

FIG. 31**FIG. 32**

LIST OF ANTIFUSE OPTION SPECIFICATIONS

SPECIFICATIONS	STATE OF ANTIFUSE			OUTPUT			
	AF0	AF1	AF2	BNK2B	BPX4	BPX8	BPX16
4Bank / x4	BREAKDOWN	NON-BREAKDOWN	BREAKDOWN	'H'	'H'	'L'	'L'
4Bank / x8	BREAKDOWN	BREAKDOWN	BREAKDOWN	'H'	'H'	'H'	'L'
4Bank / x16	BREAKDOWN	BREAKDOWN	NON-BREAKDOWN	'H'	'H'	'H'	'H'
2Bank / x4	NON-BREAKDOWN	NON-BREAKDOWN	BREAKDOWN	'L'	'H'	'L'	'L'
2Bank / x8	NON-BREAKDOWN	BREAKDOWN	BREAKDOWN	'L'	'H'	'H'	'L'
2Bank / x16	NON-BREAKDOWN	BREAKDOWN	NON-BREAKDOWN	'L'	'H'	'H'	'H'

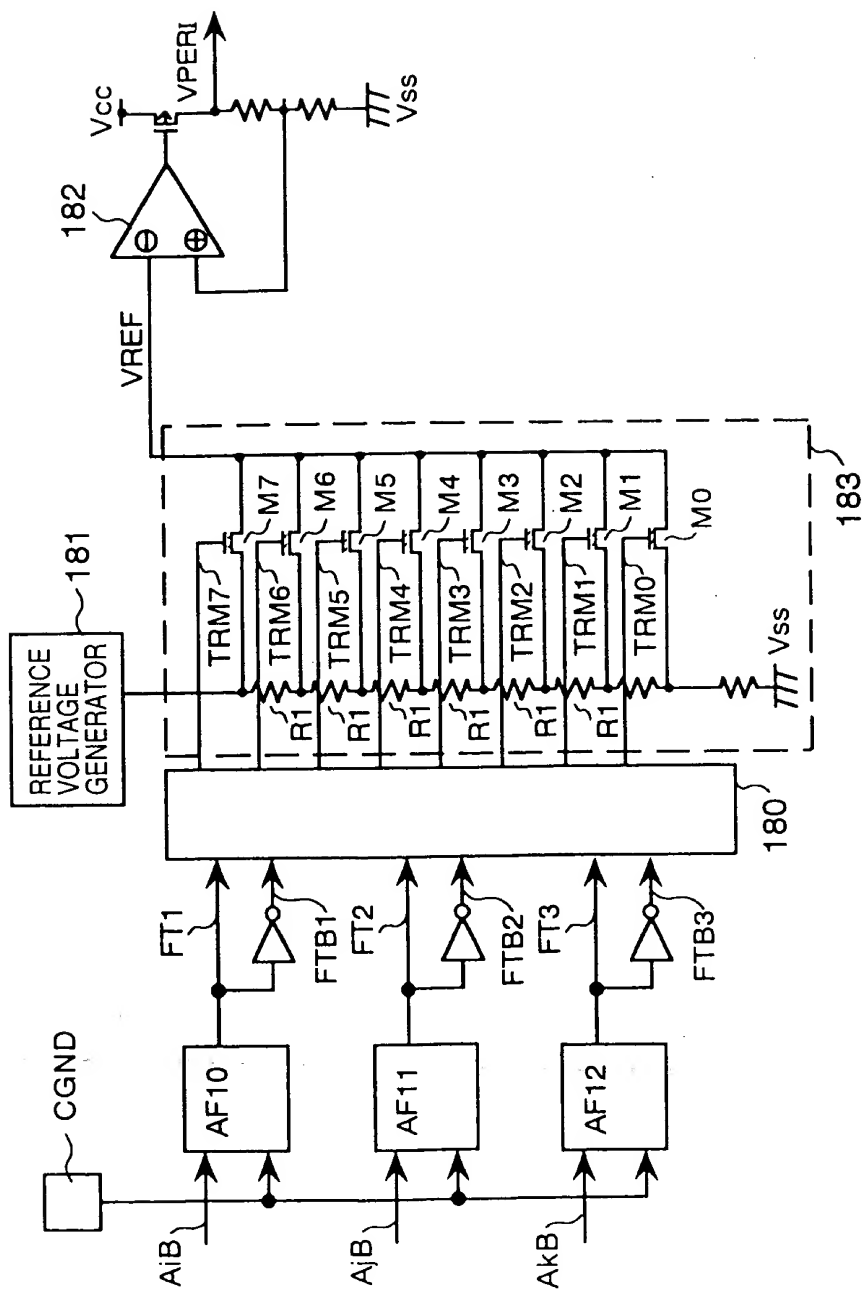


FIG. 34

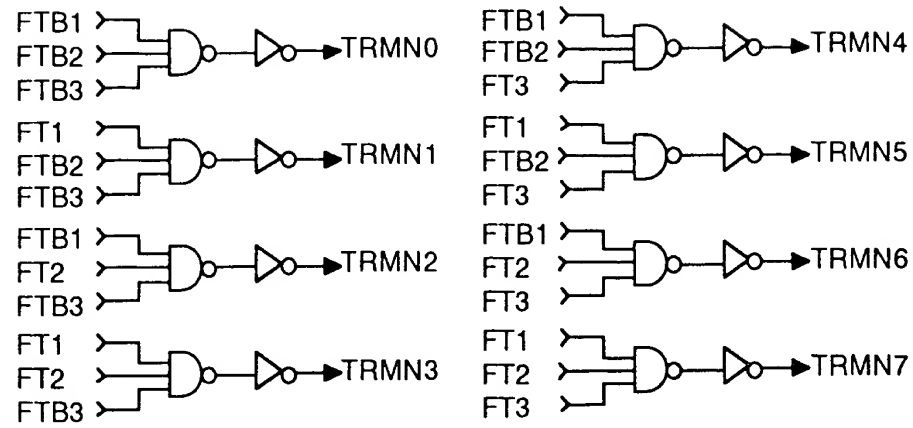


FIG. 35

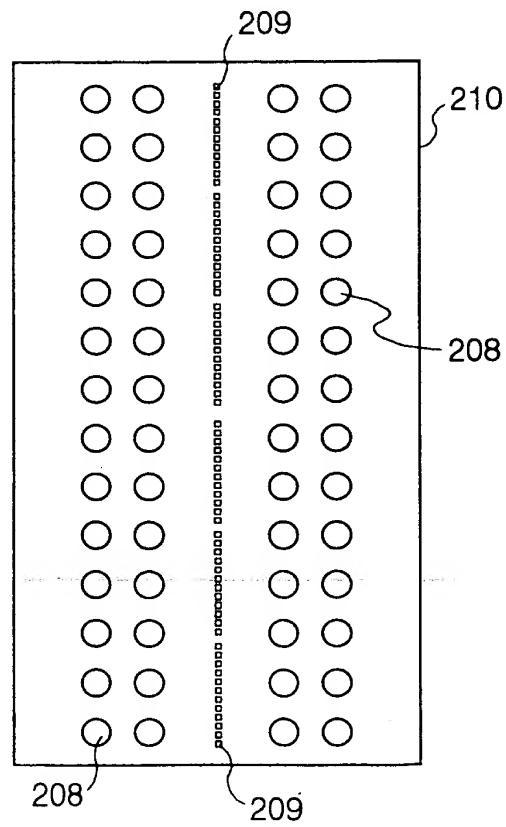


FIG. 36

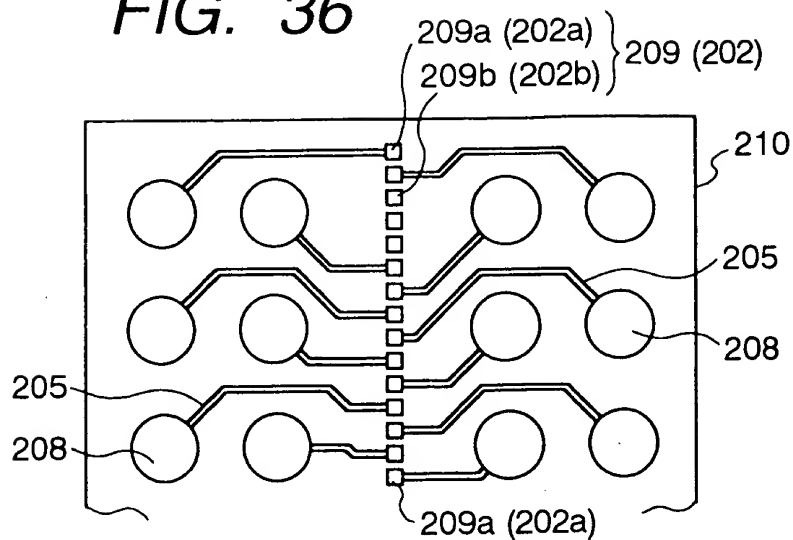


FIG. 37

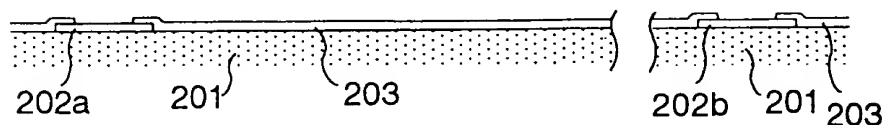


FIG. 38

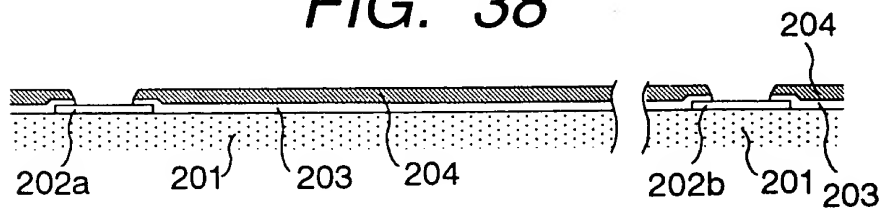


FIG. 39

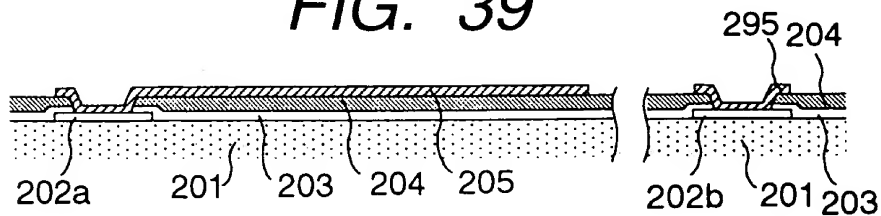


FIG. 40

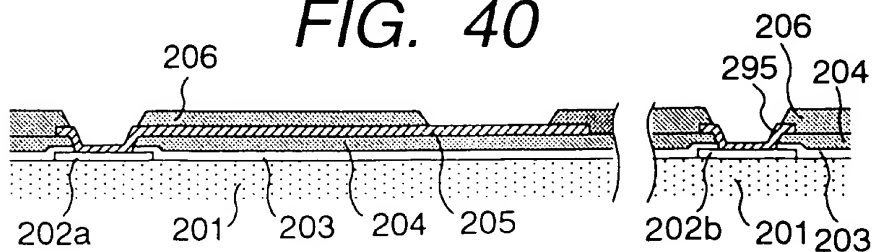


FIG. 41

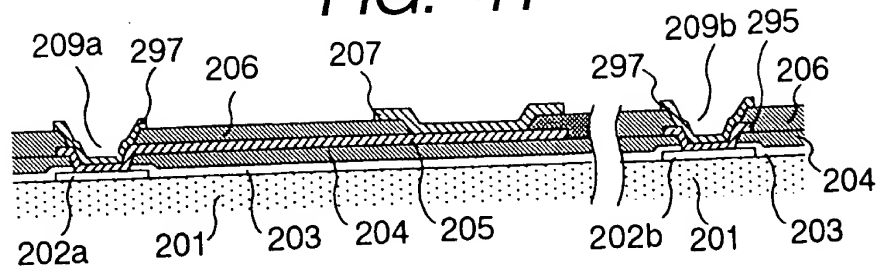


FIG. 42

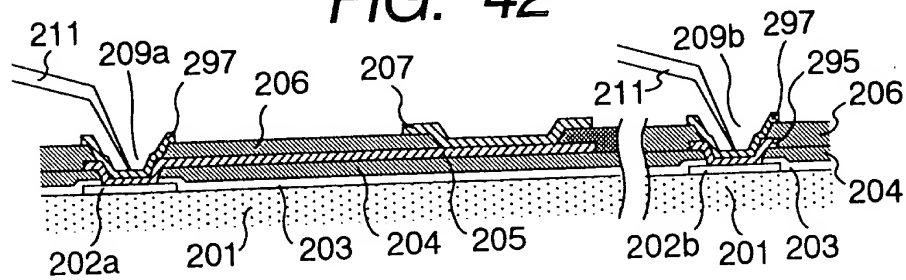


FIG. 43

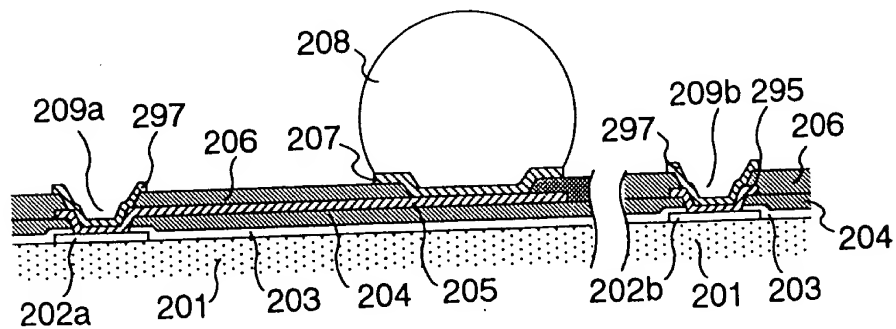


FIG. 44

CONTENTS	NUMBER OF BONDING PADS	NUMBER OF PACKAGE EXTERNAL TERMINALS
SIGNAL INPUT/OUTPUT	39	39
POWER	24	14
FUNCTION SELECTION	3	0
PROBE TEST	6	0
NON-CONNECTION	—	1
TOTAL	72	54

FIG. 45

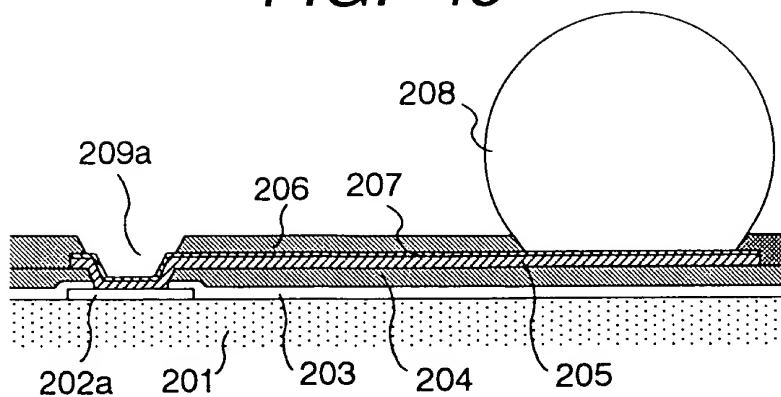


FIG. 46

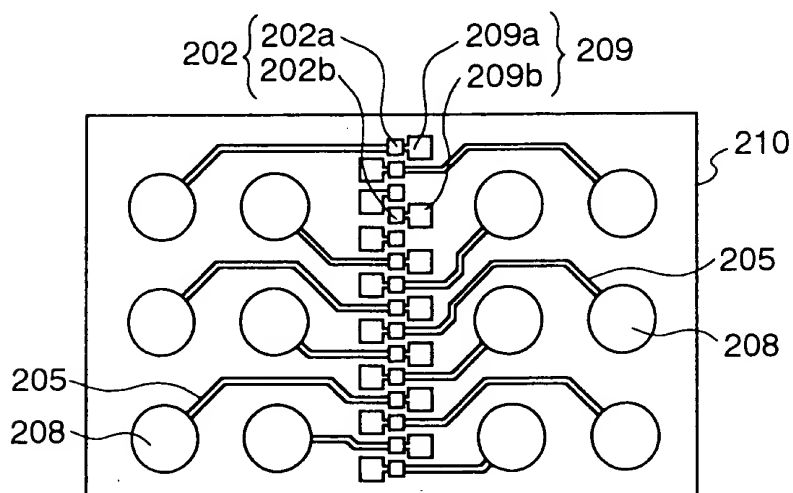
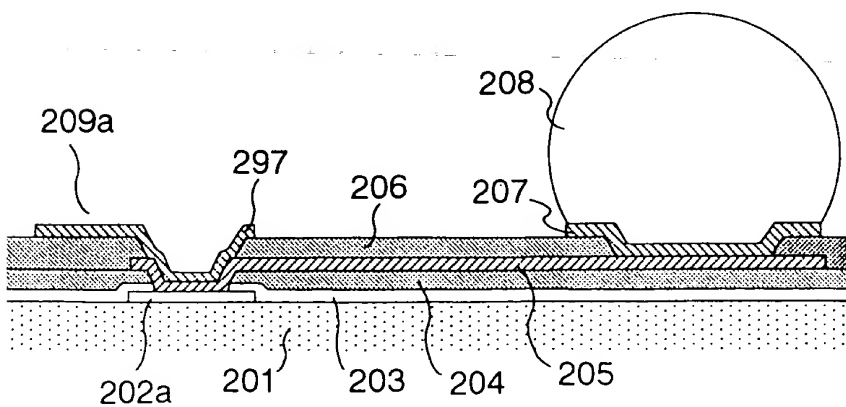


FIG. 47



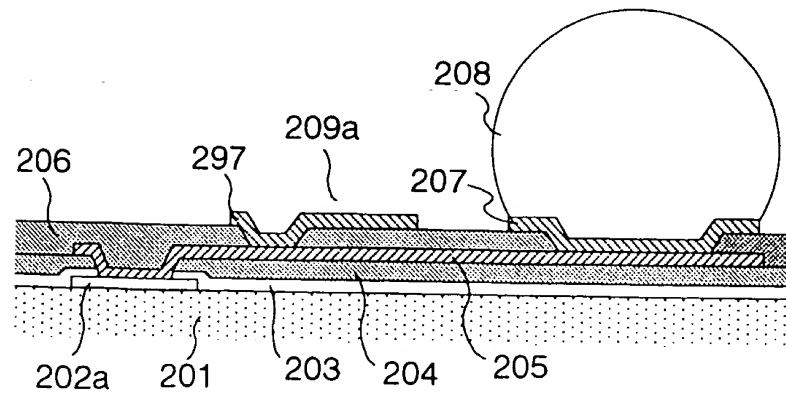
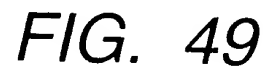


FIG. 51

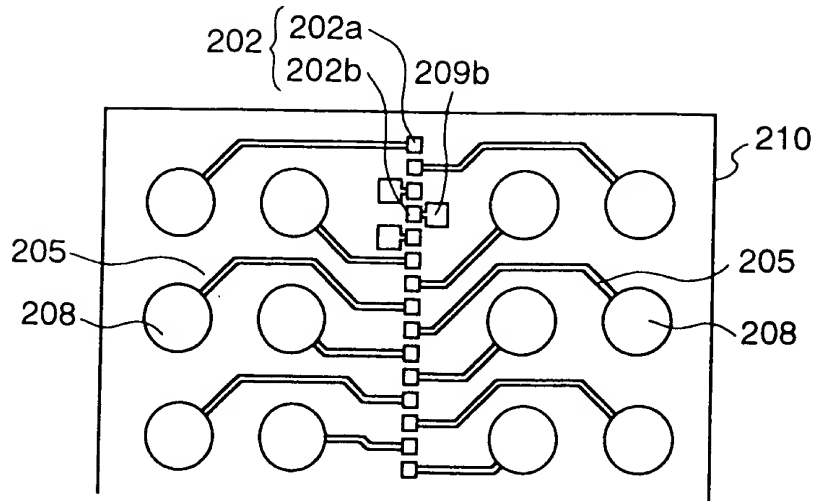
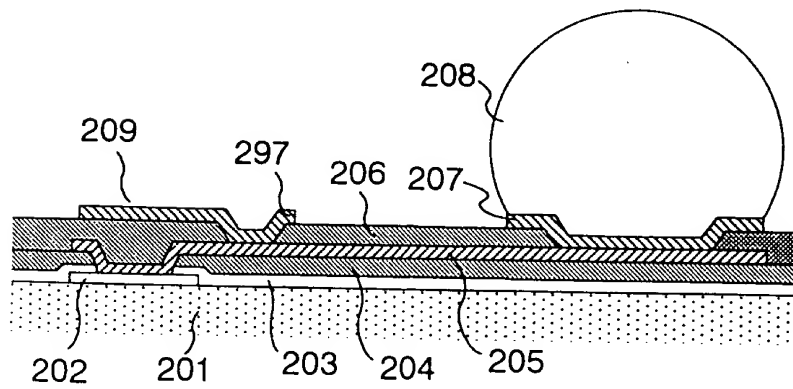


FIG. 52



A diagram showing a grid of rectangular blocks arranged in a cross-like pattern. The blocks are labeled 210 and 202. The grid is enclosed within an oval boundary labeled 220. The blocks are arranged in a 5x5 grid, with the central block labeled 202 and the surrounding blocks labeled 210.

FIG. 54

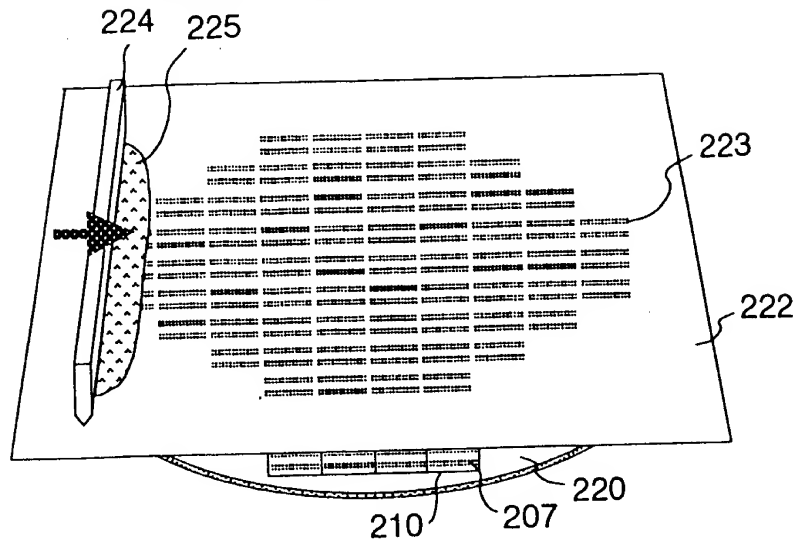
FIG. 1 is a schematic diagram of a storage device in a "formed state of order". The diagram shows a central array of memory cells (210) surrounded by a peripheral memory array (207). The entire structure is enclosed in an oval boundary (220).

FIG. 55

Figure 1 is a perspective view of a circular substrate 220. The substrate has a central rectangular region 210. Within this central region, there is a series of vertical lines 207. The substrate is covered with a grid of small circles 211. The central region 210 is surrounded by a ring of small circles 221.

FIG. 56

SOLDER BUMP FORMING PROCESS



CROSS-SECTION

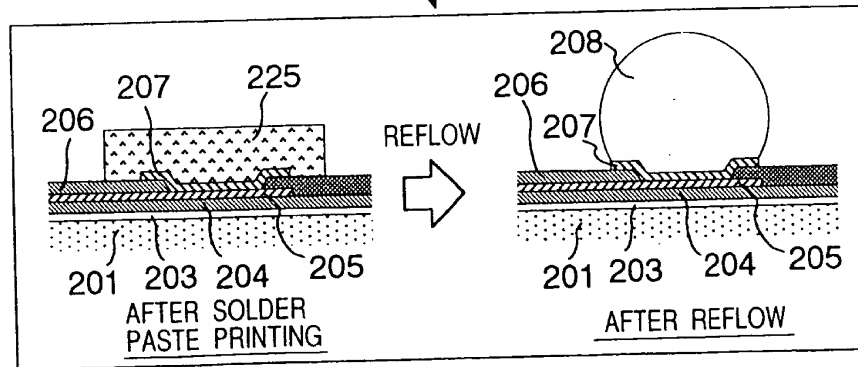


FIG. 57

PIECE CUTTING PROCESS

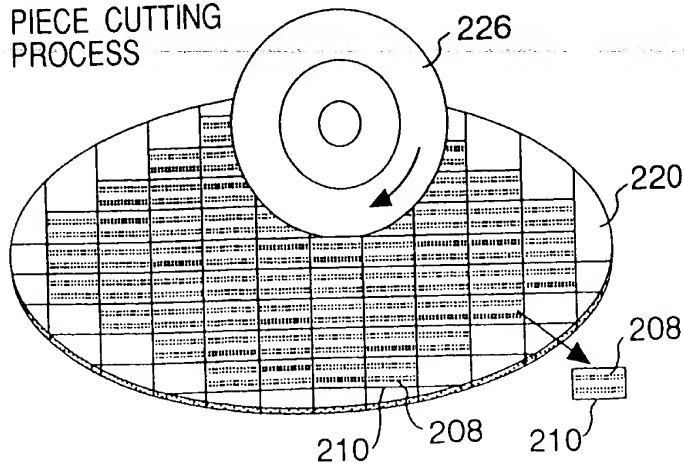


FIG. 58

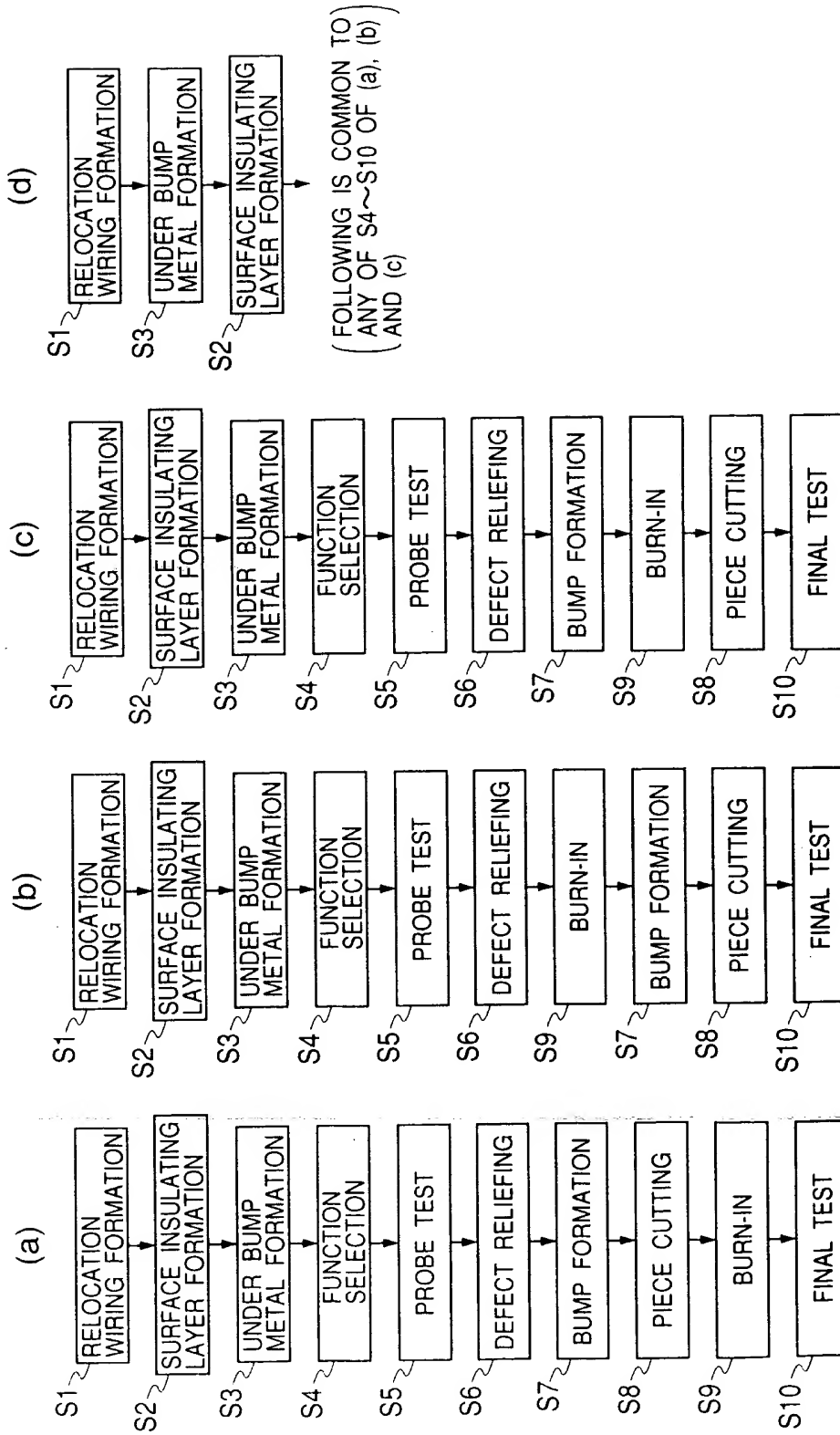


FIG. 59

PROBE IN RESPECTIVE TESTING PROCESSES,
CONTACT POINTS OF SOCKET OR THE LIKE

CONTENTS OF TERMINAL		DEDICATED FOR PROBE TEST			SUPPLY OF POWER AND INPUT/OUTPUT OF SIGNAL			CORRE- SPONDING PROCESS FLOW
CLASSIFI- CATION OF TEST		PROBE TEST	BURN-IN	FINAL TEST	PROBE TEST	BURN-IN	FINAL TEST	
MODE	1	TESTING PAD	NONUSE	NONUSE	TESTING PAD	BUMP	BUMP	a, c
	2	TESTING PAD	NONUSE	NONUSE	UNDER BUMP METAL	BUMP	BUMP	a, c
	3	TESTING PAD	NONUSE	NONUSE	TESTING PAD	TESTING PAD	BUMP	a, b, c
	4	TESTING PAD	NONUSE	NONUSE	UNDER BUMP METAL	UNDER BUMP METAL	BUMP	b

FIG. 59